Exam Solutions Mean = 54.1, Median = 56, σ = 19.9

There are 100 points over 3 problems on 3 additional pages.

Be sure to **state** any assumptions made and **check** them when possible.

Useful units and constants

Definition of electron volt: $1\ \text{eV} = 1.6 \times 10^{-19}\ \text{J}$

Electronic charge: $q = 1.6 \times 10^{-19}\ \text{C}$

Boltzmann constant: $k = 8.62 \times 10^{-5}\ \text{eV/K} = 1.38 \times 10^{-23}\ \text{J/K}$

Thermal voltage at room temperature: $kT / q = 0.0259\ \text{V}$

Relative permittivity of silicon: $\varepsilon_r = 11.7$

Relative permittivity of SiO_2: $\varepsilon_r = 3.9$

Permittivity of free space: $\varepsilon_0 = 8.854 \times 10^{-14}\ \text{F/cm}$

Silicon intrinsic carrier density at room temperature: $n_i = 10^{10}/\text{cm}^3$

Band gap for silicon: $E_G = 1.12\ \text{eV}$

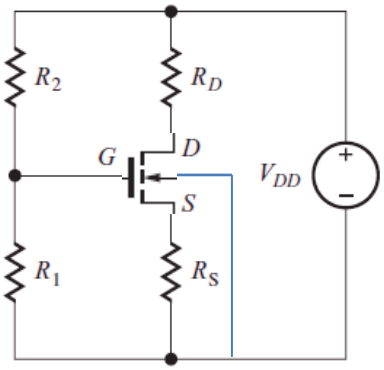
1. (32 points) Design a four-resistor bias network for an NMOS transistor with $R_D = R_S$ to give a Q-point (i_{DS}, v_{DS}) of (0.25 mA, 2 V) with $V_{DD} = 5$ V. Use $K_n' = 50$ μA/V^2, $V_{TO} = 0.8$ V, and (W/L) = 2/1. Ignore channel length modulation effect.

(a) (5 points) What are the values of R_D and R_S?

(b) (12 points) What is the ratio R_1/R_2 to give the desired biasing for $\gamma = 0$? What is transistor mode?

(c) (5 points) What value of R_1 would make the current through R_1 equal to 5% of drain current.

(d) (10 points) Repeat (b) if body effect parameter is $\gamma = 0.6$ V$^{1/2}$ and $2\varphi_F = 0.7$ V.



(a) $i_{DS} = 0.25$ mA $= (V_{DD} - v_{DS})/(R_D+R_S) = (5 - 2)/(2R_D)$, so $R_D = R_S = (3\text{ V})/[2(0.25\text{ mA})] = 6$ kΩ.

(b) Assume saturation, then $i_{DS} = (K_n'/2)(W/L)(V_{GS} - V_{TN})^2 = 0.25$ mA. $\gamma = 0$, so $V_{TN} = V_{TO} = 0.8$ V. $V_{GS} = 0.8\text{ V} + (0.25\text{ mA})/[(25\ \mu\text{A/V}^2)(2)]^{1/2} = 3.04$ V. $V_{GD} = 3.04 - 2 = 1.04\text{ V} > V_{TN} = 0.8$ V, so not saturated. Try triode instead. $i_{DS} = (K_n')(W/L)(V_{GS} - V_{TN} - V_{DS}/2)V_{DS} = 0.25$ mA. Then $V_{GS} = 0.8\text{ V} + 2/2\text{ V} + (0.25\text{ mA})/[(50\ \mu\text{A/V}^2)(2)(2\text{ V})] = 3.05$ V. $V_{GD} = 3.05 - 2 = 1.05\text{ V} > V_{TN} = 0.8$ V, so saturated is correct. $V_{GG} = 3.05 - V_{Rs} = 3.05 - 1.5 = 4.45$ V. $R_1 / R_2 = 4.55 / (5 - 4.55) = 10.1$.

(c) $V_{DD} / (R_1 + R_2) = (0.05)\ i_{DS} = 12.5$ μA. $R_1 + R_2 = 400$ kΩ, $R_1 = 400$ kΩ $(4.55 / 5) = 364$ kΩ.

(d) $V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F}\right) = 0.8 + 0.6\left(\sqrt{1.5 + 0.7} - \sqrt{0.7}\right) = 1.19\ V.$

Assume triode. $i_{DS} = (K_n')(W/L)(V_{GS} - V_{TN} - V_{DS}/2)V_{DS} = 0.25$ mA. Then $V_{GS} = 1.18\text{ V} + 2/2\text{ V} + (0.25\text{ mA})/[(50\ \mu\text{A/V}^2)(2)(2\text{ V})] = 3.44$ V. $V_{GD} = 3.44 - 2 = 1.44\text{ V} > V_{TN} = 1.19$ V, so saturated is correct. $V_{GG} = 3.44 - V_{Rs} = 3.44 - 1.5 = 4.94$ V. $R_1 / R_2 = 4.94 / (5 - 4.94) = 82.3$.

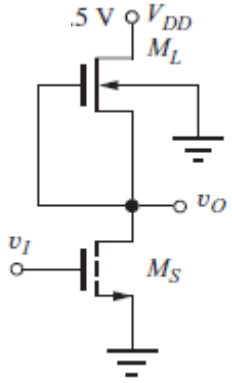
2. (36 points) An NMOS depletion load inverter design is shown in the figure below. Use K_n' = 20 μA/V^2 for both devices. V_{TO}^S = 1.0 V and V_{T0}^L = -1.0 V. Neglect the body effect.

(a) (12 pts) If $(W/L)_S$ = (1/1), find the value of $(W/L)_L$ to give V_L = 0.7 V. Neglect channel length modulation effect (λ = 0).

(b) (6 pts) How should the aspect ratios of the MOSFETs be changed to make the maximum power consumption of the inverter 4 mW, with V_H and V_L kept unchanged.

(c) (8 pts) If channel length modulation was significant, would V_L increase/decrease/stay the same (term should be included for both triode and saturation)? Explain.

(d) (10 pts) Estimate the noise margins based on the voltage transfer characteristic provided.



(a) When $V_I = V_H = V_{DD}$ = 5 V, $V_O = V_L$ =0.7 V. For M_S, V_{DS} = 0.7V, $V_{DS} < V_{GS} - V_{T0}^s$. Thus, it operates in the triode region, and I_D is expressed as:

$$I_D = K_n'\left(\frac{W}{L}\right)_s\left(V_{GS} - V_{TO}^s - \frac{V_{DS}}{2}\right)V_{DS}$$

$$I_D = 20\times 1\times\left(5-1-\frac{0.7}{2}\right)0.7 = 51.1\ \mu A$$

For load NMOS, V_{DS} = 5 - 0.7 = 4.3 V, V_{GS} = 0V. Neglecting the body effect, $V_{GS} - V_{T0}^L < V_{DS}$, so it operates in the saturation region.

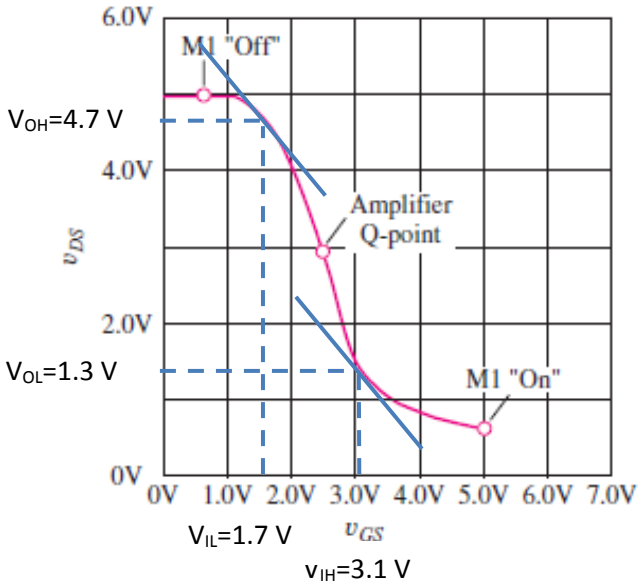
$$I_D = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (V_{GS} - V_{TO}^L)^2$$

$$\left(\frac{W}{L}\right)_L = \frac{51.1}{(20/2)\times(0+1)^2} = 5.11$$

(b) Power consumption $P_{max} = I_D V_{DD}$, I_D = 4 mW/5 V = 0.8 mA. Use the I_D expressions for switch and load transistor in (a),

M_S: $0.8\times10^3 = 20\left(\frac{W}{L}\right)_s\left(5-1-\frac{0.7}{2}\right)0.7$ => $\left(\frac{W}{L}\right)_s$ = 15.66

M_L: $0.8\times10^3 = \frac{20}{2}\left(\frac{W}{L}\right)_L (0+1)^2$ => $\left(\frac{W}{L}\right)_L = 80$



(c) If channel length modulation was significant,
For M_L in the saturation region, $V_{DS}=V_{DD}-V_L$:, $V_{DSat}=0-V_T^L$

$$I_{D\_M_L} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (0 - V_{TO}^L)^2\left[1+\lambda(V_{DD} - V_L + V_T^L)\right]$$

For M_L in the triode region, no change.

Due to the channel length modulation, drain current of M_L increases. To satisfy KCL, the drain current of M_S must also increase which requires V_{DS} of M_S to increase, V_L>0.7V.

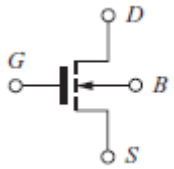
(d) Note that slope of -1 is diagonal of rectangles on grid of plot.

$NM_L = V_{IL} - V_{OL}$ = 1.7 - 1.3 = 0.4 V

$NM_H = V_{OH} - V_{IH}$ = 4.7 – 3.1 = 1.6 V

3. (32 points) Use $K_{n,p}$= 100 μA/V^2, γ = 0, and λ = 0. The on voltages of body pn junctions are 0.7 V.

(a) (10 points) $V_S = V_B$ = 2 V. V_D = 3 V. V_{T0} = 0.5V. The current **into** terminal D is 2 mA. What is V_G?



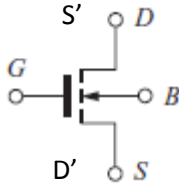
γ = 0, so no body effect. $V_{TN} = V_{T0}$ = 0.5 V. Guess in triode,

$$I_D = K_n\left(V_{GS} - V_{TN} - \frac{1}{2}V_{DS}\right)V_{DS}$$

$$2\text{ mA} = \left(100\frac{\mu A}{V^2}\right)\left(V_{GS} - 0.5\text{ V} - \frac{1}{2}1\text{ V}\right)1\text{ V}$$

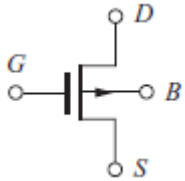
Solving, $V_{GS} = 21$ V, $V_G = V_{GS} + V_S = 23$ V. $V_{GS} - V_{TN} = 20.5\text{ V} \gg V_{DS}$, so triode is correct.

(b) (12 points) The current **into** terminal D is -2 mA. V_{T0}=0.5V. $V_S = V_B = V_G$ = 0V. Find V_D and current **into** terminal S.



I_D is negative, so electrons in channel are flowing from terminal D to S. Thus terminal D is actually the source, call it S'. $V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{S'B} + 2\varphi_F} - \sqrt{2\varphi_F}\right)$, but $\gamma = 0$, so $V_{TN} = V_{TO} = 0.5$ V. $V_{DS'} = V_{GS'} \gg V_{GS'} - V_{TN}$, so NMOS is in saturation. We first assume $I_{D'} = -I_D = \frac{K_n}{2}(V_{GS'} - V_{TN})^2 = \frac{K_n}{2}(-V_{S'} - V_{TN})^2$, $V_D = V_{S'} = -4.97$ V, check $V_{GS'} \gg V_{TN}$ and $V_{DS'} \gg V_{GS'} - V_{TN}$. However, $V_{BD} = V_{BS'} = 4.97\text{ V} \gg V_{on} = 0.7$ V, V_{on} is for the body to source (D) diode. Thus, this diode is on and $V_D = -0.7$ V, $V_{GS'} = 0.7$ V, $I_{D'} = \frac{K_n}{2}(V_{GS'} - V_{TN})^2 = 2$ μA.

(c) (10 points) This transistor is a depletion mode PMOS devices with V_{TO} = 0.5 V. $V_S = V_B$ = 0 V, V_G = -1 V, and V_D = -2 V. What mode is device operating in? What is current **into** terminal D?



$V_{TP} = V_{TO} = 0.5$ V. $V_{DS} = -1\text{ V} < V_{TP}$, so on. $V_{DS} = -2\text{ V} < V_{GS} - V_{TP} = -1.5$ V, so PMOS is in saturation. $I_D = \frac{K_p}{2}(V_{GS} - V_{TP})^2$. Solving, $I_D = 0.1125$ mA, but current **into** terminal D is -0.1125 mA.