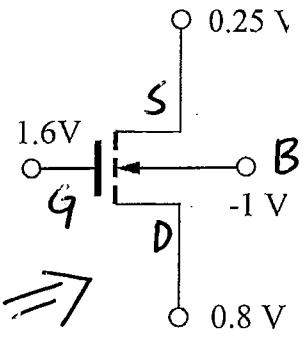
Spring 2014 Exam 2 Version A

1. For this problem, use $V_{TN} = 0.8$ V and $K_n' = 200\ \mu A/V^2$ (40 points).

(a) Identify and label the Drain (D), Source (S), Gate (G), and Bulk/Body (B) terminals of the device at right. Then, given that $W/L = 1$, $\gamma = 0.5\ V^{1/2}$ and $\lambda = 0.1\ V^{-1}$, determine the region of operation of the device and find the current flowing from D to S. Be clear and show all work to justify your answer. (20)



For NMOS $V_{DS} > 0$ ⇒

$$V_{TN} = V_{TN0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

$$= 0.8V + 0.5\left(\sqrt{(0.25-(-1)) + 0.8} - \sqrt{0.8}\right) = 1.07\ V$$

$$V_{GS} = 1.6V - 0.25V = 1.35\ V > V_{TN} \Rightarrow On$$

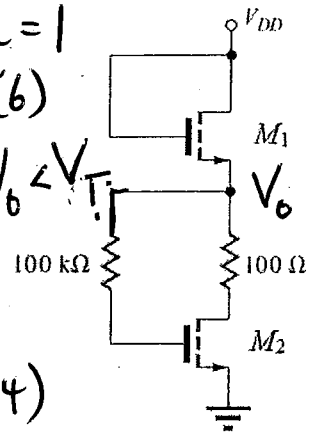
$$V_{DS} = 0.8 - 0.25V = 0.55V > V_{DSat} = V_{GS} - V_T = 1.35 - 1.07 = 0.28V$$

Saturated $I_{DS} = \frac{K_n}{2}(V_{GS}-V_T)^2\left[1+\lambda(V_{DS}-V_{DSat})\right] = \frac{200\mu A}{2V^2}(0.28V)^2\left(1+\frac{0.1}{V}(0.27V)\right)$

$= 8.05\mu A$ $K_n = K_n'$ since $W/L = 1$

(b) For the enhancement-mode NMOS devices M_1 and M_2 in circuit at right, ignore channel length modulation and body effect. $V_{DD} = 5$ V, $(W/L)_{M1} = 5/1$, $(W/L)_{M2} = 2/1$. (6)

What is the region of operation of M_1? Explain.



M_1 in Saturation $V_{GS} > V_T$, since if off no current so M_2 off ⇒ $V_o < V_T$

$V_{DS} = V_{GS} > V_{GS} - V_T = V_{DSat}$ since $V_T > 0$

Assuming M_2 is in saturation region, find the drain currents through M_1 and M_2. (14)
Based on your calculations, state whether this assumption is correct.

$$I_{DS}' = I_{DS}^2 \Rightarrow \frac{K_n'}{2}\left(\frac{W}{L}\right)_{M_1}(V_{DD}-V_o-V_T)^2 = \frac{K_n'}{2}\left(\frac{W}{L}\right)_{M_2}(V_o-V_T)^2$$

$$5(5-V_o-0.8)^2 = 2(V_o-0.8)^2$$

$$(4.2-V_o)^2 = (0.4)(V_o-0.8)^2$$

$$4.2 - V_o = \pm\sqrt{0.4}(V_o-0.8)$$ (>0)

$$4.2 + \sqrt{0.4}(0.8) = (1+\sqrt{0.4})V_o$$

$$V_o = \frac{4.706V}{1.632} = 2.88V$$

$$I_{DS}' = 5(4.2-2.88)^2\frac{200\mu A}{2V^2}$$

$$= 871\mu A$$

$$V_{DS}^2 = V_o - I_{DS}'(100\Omega)$$

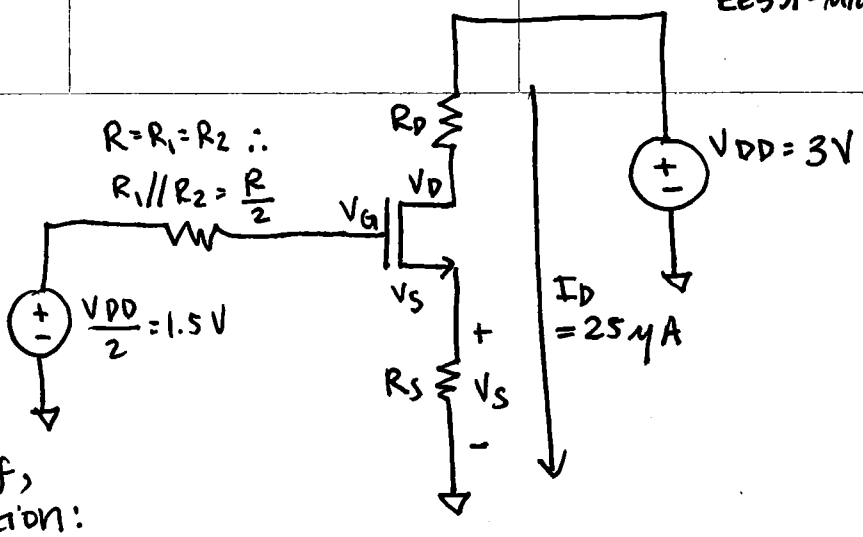
$$= 2.88V - 0.09V = 2.79V$$

$$> V_{GS} - V_T = V_{DS}^{sat} = 2.08V$$

so assumption checks

Problem 2.

Redraw circuit:



a)

Assume not cutoff,
First try saturation:

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TO})^2 \Rightarrow 25\mu A = \frac{200\frac{\mu A}{V^2}}{2}(V_{GS} - 0.8)^2$$

$\therefore V_{GS} = 1.3\ V$ Check conditions:

$V_{GS} > V_{TO}$ ✓

$V_{DS} > V_{GS} - V_T$

$(= 1 > 1.3 - 0.8)$ ✓

Show it doesn't work for Triode:

$$I_D = K_n(V_{GS} - V_{TO})V_{DS} - \frac{V_{DS}^2}{2}$$

$$\Rightarrow 25\mu A = 200\frac{\mu A}{V^2}(V_{GS} - 0.8\ V)(1V) - \frac{(1V)^2}{2}$$

$\therefore V_{GS} = 1.425\ V$ Check conditions:

$V_{GS} > V_{TO}$ ✓

$V_{DS} < V_{GS} - V_T$ NO?

$(= 1 < 1.425 - 0.8)$

not true!

∴ saturation mode

b) KVL: $V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

① $\frac{V_{DD} - V_{DS}}{I_D} = R_D + R_S \rightarrow \frac{3-1\,V}{25\mu A} = 80\,k\Omega$

From a) $V_{GS} = 1.3\,V$, $V_G = V_{DD}/2 = 1.5\,V$

$V_{GS} = V_G - V_S = V_G - I_D R_S$

$\rightarrow R_S = \frac{V_G - V_{GS}}{I_D} = \frac{1.5-1.3\,V}{25\mu A} = \frac{0.2\,V}{25\mu A} =$ **$8\,k\Omega = R_S$**

Plug R_S into ①:

$\rightarrow R_D + 8\,k\Omega = 80\,k\Omega \rightarrow$ **$72\,k\Omega = R_D$**

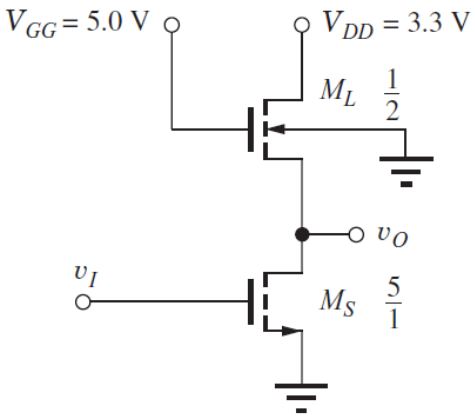
c) Let $R_1 = R_2 = R$

KVL: $V_{DD} - 0.05 \times I_D R_1 - 0.05 \times I_D R_2 = 0$

$V_{DD} - 0.1 \times I_D R = 0$

$\rightarrow R = \frac{V_{DD}}{0.1 \times I_D} = \frac{3V}{0.1 \times 25\mu A} =$ **$1.2\,M\Omega = R_1 = R_2 = R$**

3. (30 pts) An NMOS linear load inverter design is shown in the figure to the right. Use the following parameters for both devices: V_{TO} = 0.8 V, K_n' = 200 μA/V^2.



(a) Find V_H and V_L. Ignore channel length modulation and body effect. [15]

$$V_H = V_{DD} = 3.3\text{V};$$

When $v_I = V_H$ and v_O is low (v_L), M_S and M_L are both in the triode region and the i_D values are given by:

$$i_{DSS} = K_n'\left(\frac{W}{L}\right)_s\left(v_{GSS} - V_{TNS} - \frac{v_{DSS}}{2}\right)v_{DSS}$$

$$i_{DSL} = K_n'\left(\frac{W}{L}\right)_L\left(v_{GSL} - V_{TNL} - \frac{v_{DSL}}{2}\right)v_{DSL}$$

Equating the two:

$$\left(\frac{1}{2}\right)\left(5.0 - v_L - 0.8 - \frac{3.3 - v_L}{2}\right)(3.3 - v_L) = 5\left(3.3 - 0.8 - \frac{v_L}{2}\right)v_L$$

Solving for v_L gives v_L = 0.305V

(b) If body effect exists (γ > 0), will V_H increase/decrease/stay the same? How about V_L? Explain. [5]

Only the load device has body effect. V_H is unaffected by the body effect unless V_{TNL} becomes larger than 1.7 V so that M_L is off when v_0 equals V_{DD}. This would require an extremely large value of the body effect coefficient, since V_{TNL0} is just 0.8 V. Thus no change is expected.

The body effect will cause an increase in V_{TNL} and thus a decrease in i_{DSL} which makes V_L decrease to match currents. However, the change is expected to be small as V_{SBL}=V_L is small.

(c) Design a gate to perform function $\overline{A \cdot (B + C)}$ based on this inverter with the same V_L and V_H and noise margins and performance. Sketch your design and specify W/L ratios for all transistors. [10]

Load is unchanged. W/L ratios for switching (pull-down) transistors are chosen based on worst case. Weakest pull-down is when B or C and A are on. Conducting path to ground is via B and A or C and A, so these transistors need double width to compensate for double length. Thus W/L values should be 10/1.