Name:_____ Student Number:_____

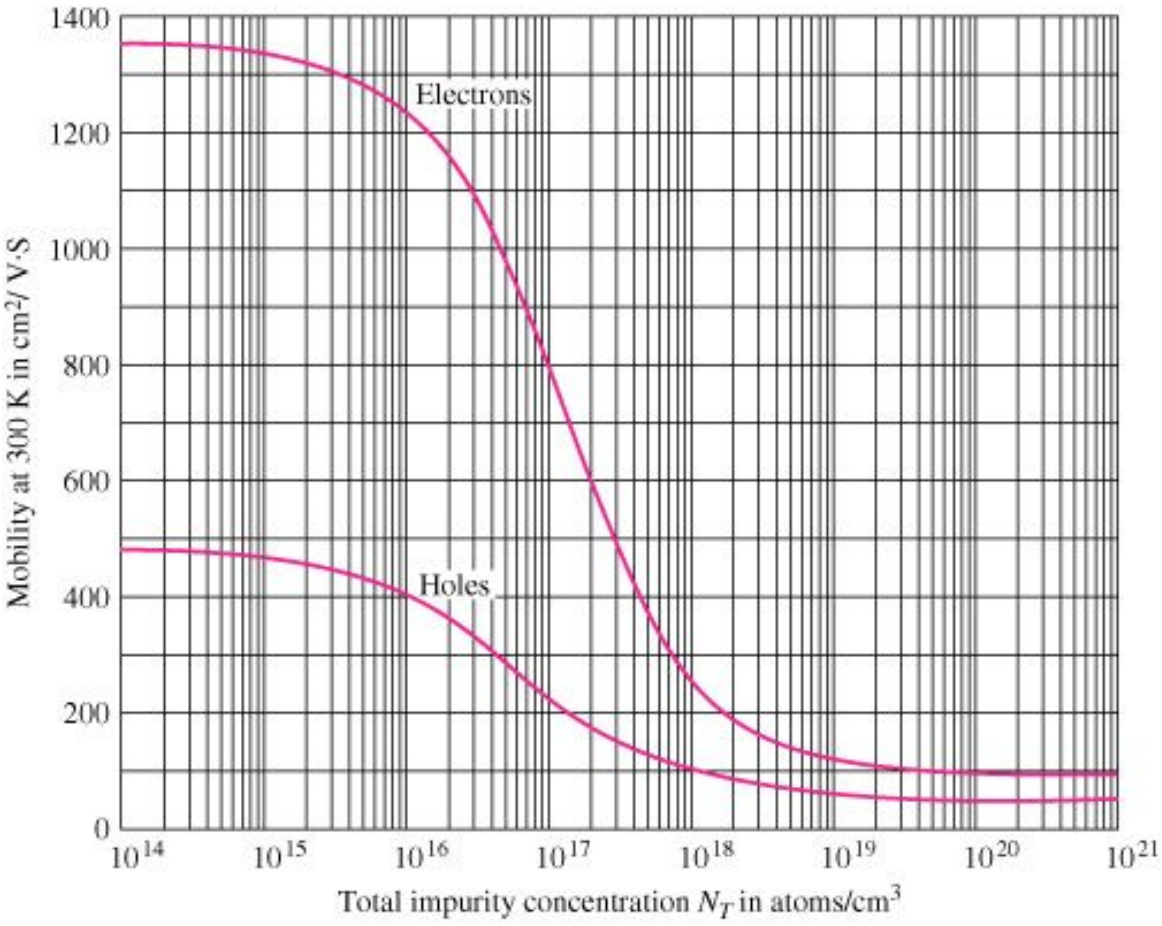
There are 200 points over 6 problems on 6 additional pages.

Be sure to **state** any assumptions made and **check** them when possible.

Useful units and constants

Definition of electron volt: 1 eV = 1.6×10^{-19} J
Electronic charge: $q = 1.6 \times 10^{-19}$ C
Boltzmann constant: $k = 8.62 \times 10^{-5}$ eV/K = 1.38×10^{-23} J/K
Thermal voltage at room temperature: $kT / q = 0.0259$ V
Relative permittivity of silicon: $\varepsilon_r = 11.7$
Relative permittivity of SiO_2: $\varepsilon_r = 3.9$
Permittivity of free space: $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm
Silicon intrinsic carrier density at room temperature: $n_i = 10^{10}/cm^3$
Band gap for silicon: $E_G = 1.12$ eV

Default MOS parameters: $K_n' = 200$ μA/V^2, $K_p' = 100$ μA/V^2, $V_{TN0} = 0.5$ V, $V_{TP0} = -0.5$ V, $V_{TD0} = -2$ V, $\gamma = 0.5$ V$^{1/2}$, $|2\varphi_F| = 0.6$ V, $\lambda = 0$, $(W/L) = 1$
Default diode parameters: $I_s = 10^{-16}$ A, $n = 1$, $V_{Zener} = 5$ V, $R_{Zener} = 0$.



1. [36 points] A silicon pn junction has uniform doping concentrations of $N_A = 10^{17}/cm^3$ and $N_D = 5\times10^{18}/cm^3$ on the two sides of the junction, respectively. Both sides are narrow with undepleted region widths of W_p'=200 nm and W_n'=50 nm. The minority carrier lifetimes are $\tau n_p = 2$ μs and $\tau p_n = 0.1$ μs. The diode has a cross sectional area of 200 nm × 500 nm.

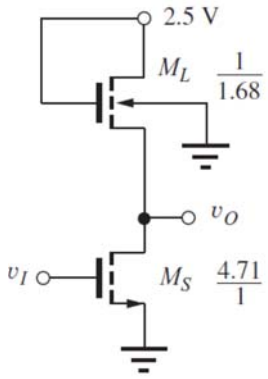
a) [10] Calculate the reverse leakage current I_S.

b) [8] What is the change in depletion charge as the voltage changes from 0 to 0.7 V?

c) [8] What is the change in diffusion charge (stored minority charge) as the voltage changes from 0 to 0.7 V?

d) [10] If the diode was operated with forward currents on the order of 1 μA, what would be an appropriate Thevenin equivalent linear model?

2. [40 points] For the inverter shown to the right, use MOS parameters on cover page.



(a) [10] Calculate V_H.

(b) [10] Calculate V_L.

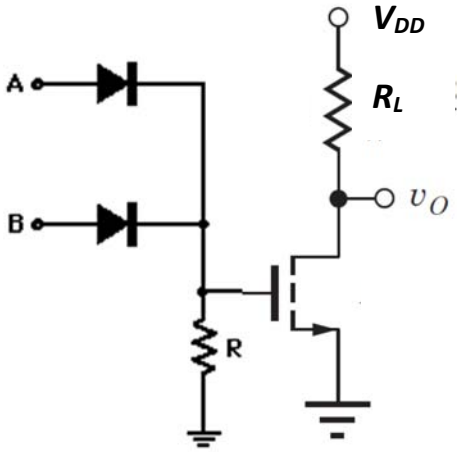
(c) [8] Calculate V_{IL}.

(d) [12] Calculate t_{pLH} for step function input (V_H to V_L at t=0) and total load capacitance of 5 pF. Use method introduced in lecture.

3. [30 points] In the circuit to the right, V_{DD} = 3 V, R_L = 1 kΩ, R = 20 kΩ, and V_{on} = 0.7 V. Use default MOS parameters (cover page).

(a) [15] Sketch v_O versus v_A for v_B = 0 and for $v_B = V_{DD}$ (two lines). What function does this circuit implement?

(b) [15] Calculate V_L and V_H and indicate on the plot in (a).



4. [34 points] Design a CMOS gate that implements the logic function $Z = \bar{A} + \bar{B} \cdot (C + \bar{D})$. Assume both inverted and noninverted logic signals are available.

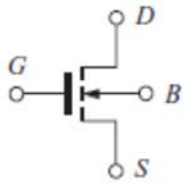
(a) [12] Draw the CMOS circuit design.

(b) [12] Design the aspect ratios for all transistors to make worst case VTC and switching speed equivalent to inverter with (W/L) for nMOS of (1/1) and (W/L) for pMOS of (2/1).

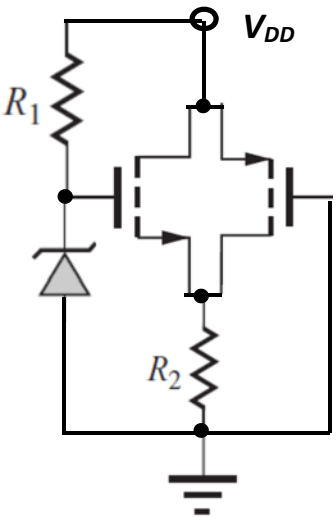
(c) [10] For your design, calculate the worst-case initial (just after input switches between V_H and V_L) pull-up current for V_{DD} = 1.5 V. Use $\gamma = 0$ (or $\alpha = 0.2$ for 5 points bonus credit).

5. [30 points] For problems below, use parameters on cover page, except assume $\gamma = 0$.

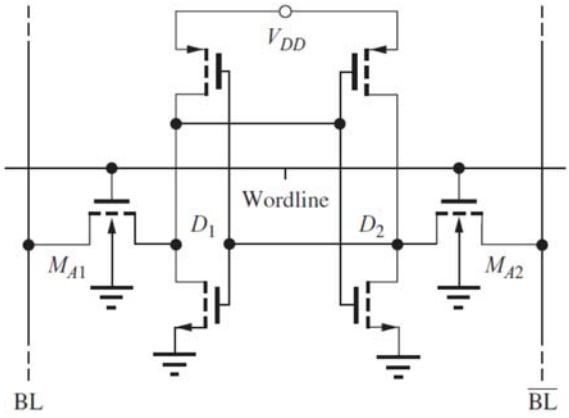
(a) [10] $V_S = 0$ V and $V_D = 2$ V. The current **into** terminal D is 2 mA. Find V_G. What mode is transistor operating in?



(b) [20] $V_{DD} = 10$ V, $R_1 = 50$ kΩ, and $R_2 = 10$ kΩ. $(W/L) = 1$ for both transistors. Determine the mode of each transistor and the voltage across resistor R_2.



6. [30 points] In the SRAM cell to the right, V_{DD} = 2 V. Use MOS parameters on cover page, except use assume γ = 0.



(a) [15] V_{D1} = 2 V, V_{D2} = 0 V, and both bitlines are precharged to 1 V. What would be the initial current **into** each bit line (BL and $\overline{BL}$) immediately after the wordline voltage is switched from 0 to 2 V?

(b) [15] Initially, V_{D1} = 2 V and V_{D2} = 0 V. If the bit line voltages are held to $V_{BL} = 0$ V and $V_{\overline{BL}} = 0$ V and the wordline at 2 V, what is the final steady-state value for V_{D1} if V_{D2} remains near 0 V?