Name: Solutions **Student Number:** ____________

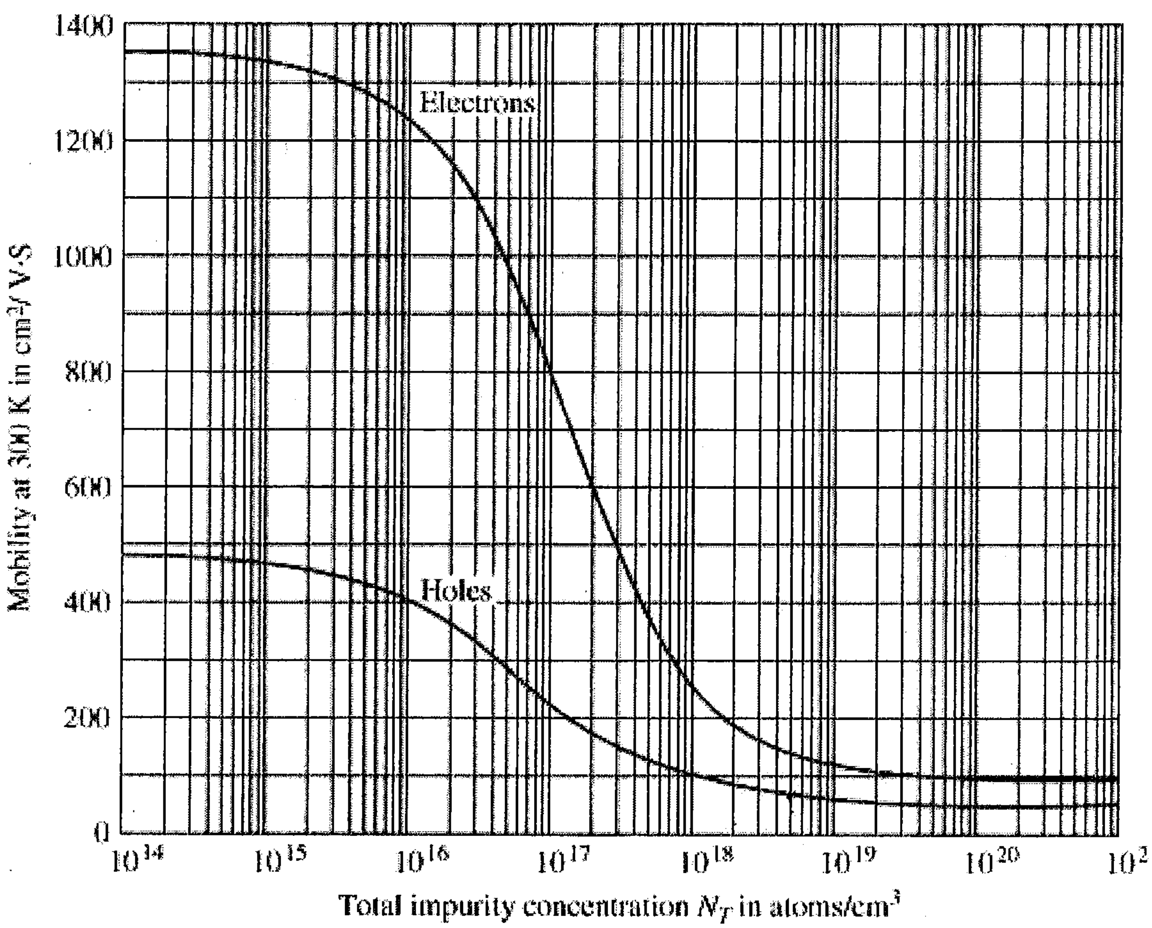
There are 200 points over 6 problems on 6 additional pages.

Be sure to **state** any assumptions made and **check** them when possible.

Useful units and constants

Definition of electron volt: $1\text{ eV} = 1.6 \times 10^{-19}$ J
Electronic charge: $q = 1.6 \times 10^{-19}$ C
Boltzmann constant: $k = 8.62 \times 10^{-5}$ eV/K $= 1.38 \times 10^{-23}$ J/K
Thermal voltage at room temperature: $kT / q = 0.0259$ V
Relative permittivity of silicon: $\varepsilon_r = 11.7$
Relative permittivity of SiO_2: $\varepsilon_r = 3.9$
Permittivity of free space: $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm
Silicon intrinsic carrier density at room temperature: $n_i = 10^{10}/\text{cm}^3$
Band gap for silicon: $E_G = 1.12$ eV

Default MOS parameters: $K_n' = 200\ \mu\text{A/V}^2$, $K_p' = 100\ \mu\text{A/V}^2$, $V_{TN0} = 0.5$ V, $V_{TP0} = -0.5$ V, $V_{TD0} = -2$ V, $\gamma = 0.5\ \text{V}^{1/2}$, $|2\varphi_F| = 0.6$ V, $\lambda = 0$, $(W/L) = 1$
Default diode parameters: $I_s = 10^{-16}$ A, $n = 1$, $V_{Zener} = 5$ V, $R_{Zener} = 0$.



1. [36 points] A silicon pn junction has uniform doping concentrations of $N_A = 10^{17}/\text{cm}^3$ and $N_D = 5\times10^{18}/\text{cm}^3$ on the two sides of the junction, respectively. Both sides are narrow with undepleted region widths of W_p'=200 nm and W_n'=50 nm. The minority carrier lifetimes are $\tau n_p = 2$ µs and $\tau p_n = 0.1$ µs. The diode has a cross sectional area of 200 nm × 500 nm.

a) [10] Calculate the reverse leakage current I_S.

b) [8] What is the change in depletion charge as the voltage changes from 0 to 0.7 V?

c) [8] What is the change in diffusion charge (stored minority charge) as the voltage changes from 0 to 0.7 V?

d) [10] If the diode was operated with forward currents on the order of 1 µA, what would be an appropriate Thevenin equivalent linear model?

$D_{np} = (0.026V)(800 \frac{cm^2}{V\cdot s})$ $N_A = 10^{17}$

$D_{pn} = (0.026V)(95 \frac{cm^2}{V\cdot s})$ $N_D = 5\times10^{18}$

(a) $I_s = qAn_i^2\left[\frac{D_{np}}{N_a W_p} + \frac{D_{pn}}{N_d W_n}\right]$

$= (1.6\times10^{-19}C)(200\times10^{-7}cm \cdot 500\times10^{-7}cm)(10^{20}cm^{-6})\left[\frac{20.8\ cm^2/s}{10^{17}cm^{-3}\ 200\times10^{-7}cm} + \frac{2.5\ cm^2/s}{5\times10^{18}\times5\times10^{-6}}\right]$

$= \underline{1.66\times10^{-18}\ A}$

$\varphi_i = \frac{kT}{q}\ln\left(\frac{10^{17}\ 5\times10^{18}}{10^{20}}\right) = 0.94V$

(b) $|Q_d| = A\sqrt{2K_s\epsilon_0 qN_a(\varphi_i - V_a)}$

$\Delta Q_d = \left[(2\times11.7\times8.854\times10^{-14}\frac{F}{cm})(1.6\times10^{-19}C)(10^{17})\right]^{1/2}\left[(0.24)^{1/2} - (0.94)^{1/2}\right]$

$= (1.82\times10^{-7}C/cm^2)(10^{-9}cm^2)(-0.48)$

$= -0.87\times10^{-16}C$

(c) $Q_{diff} = qAn_i^2\left[\frac{W_p}{2N_a} + \frac{W_n}{2N_d}\right](e^{qV_a/kT} - 1)$

$= (1.6\times10^{-19}C)(10^{-9}cm^2)(10^{20}cm^{-6})\left(\frac{2\times10^{-5}cm}{2\times10^{17}cm^{-3}} + \frac{5\times10^{-6}}{10^{19}cm^{-3}}\right)$

$\Delta Q_{diff} = 1.6\times10^{-30}C\left(e^{0.7/0.026} - 1\right) = 7.9\times10^{-19}C$

(d) $V_{th} = \frac{kt}{q}\ln\left(\frac{I}{I_s}\right) = (0.026V)\ln\left(\frac{10^{-6}}{1.66\times10^{-18}}\right) = 0.705V$

$\frac{dI}{dV} = \frac{I}{kT/q} = 10^{-6}/.026V = \frac{1}{26k\Omega} = \frac{1}{R_{th}}$

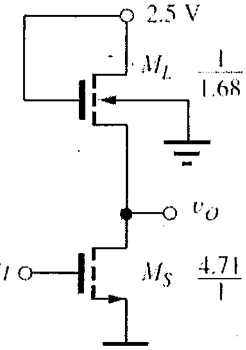
2. [40 points] For the inverter shown to the right, use MOS parameters on cover page.

(a) [10] Calculate V_H.

(b) [10] Calculate V_L.

(c) [8] Calculate V_{IL}.

(d) [12] Calculate t_{pLH} for step function input (V_H to V_L at t=0) and total load capacitance of 5 pF. Use method introduced in lecture.



(a) For V_H $V_{in} = V_L$, assume $V_L < V_{TNS} \Rightarrow M_s$ off

$V_H = 2.5V - V_{TL}$ $V_{TL} = V_{TNO} + \gamma\left(\sqrt{V_H + 2\phi_F} - \sqrt{2\phi_F}\right)$

Can solve, but easier to guess & iterate. $= 0.5V + 0.5V^{1/2}\left(\sqrt{V_H + 0.6V} - \sqrt{0.6V}\right)$

Guess $V_{TL} = 1V \Rightarrow V_H = 1.5V \Rightarrow V_{TL} = 0.84V \Rightarrow V_H = 1.66V$

$\Rightarrow V_{TL} = 0.86V \Rightarrow \underline{V_H = 1.64V} \Rightarrow V_{TL} = 0.86V$ converged

(b) $V_{in} = V_H = 1.64V$ Assume M_S linear, M_L sat Guess $V_{TL} \cong 0.6V$

$$\frac{\cancel{K_n'}}{2}\left(\frac{W}{L}\right)_L \left(V_{GS}^L - V_{TL}\right)^2 = \cancel{K_n'}\left(\frac{W}{L}\right)_S\left(V_{GS}^S - V_{TS} - \frac{V_L}{2}\right)V_L$$

$$(2.5V - V_L - V_{TL})^2 = \underbrace{2(4.71)(1.68)}_{15.83}\left(1.64 - 0.5V - \frac{V_L}{2}\right)V_L$$

$\Rightarrow \underline{V_L = 0.188V}$, $V_{TL} = 0.55V$ after solving $V_L = V_{DS} < V_{DSsat} = 1.64 - 0.5 = 1.14V$

(c) For V_{IL}, $\frac{dV_O}{dV_I} = -1$. For saturated load, this occurs as soon as M_S turns on ($V_I = V_{TN} = 0.5V$) $\underline{V_{IL} = 0.5V}$

no body effect for M_S since $V_{SB} = 0$

(d) For τ_{PLH} V_O goes from $V_L = 0.188V$ to $\frac{V_L + V_H}{2} = 0.914V$

$\Delta V = 0.726V$, M_S off, M_L saturated

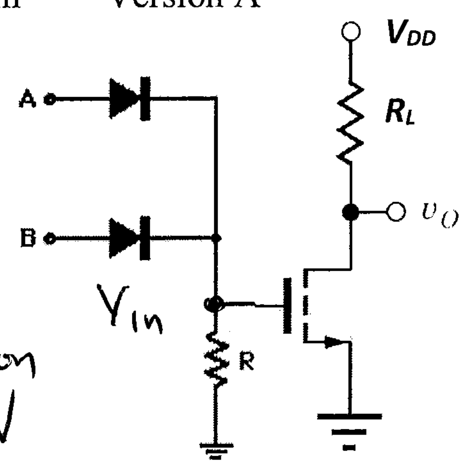
$$I_L = I_C = \frac{200\mu A/V^2}{2(1.68)}\left(2.5 - V_O - V_{TL}(V_O)\right)^2 = \begin{cases} 185\mu A & \text{for } V_O = 0.188V,\ V_{TL} = 0.55V \\ 43.6\mu A & \text{for } V_O = 0.914V,\ V_{TL} = 0.73V \end{cases}$$

$$\tau_{PLH} = \frac{C\Delta V}{I_{avg}} = \frac{(5\times10^{-12}F)(0.726V)}{0.5(154+37)10^{-6}A} = 3.8\times10^{-8}s = 38ns$$

3. [30 points] In the circuit to the right, $V_{DD} = 3$ V, $R_L = 1$ kΩ, $R = 20$ kΩ, and $V_{on} = 0.7$ V. Use default MOS parameters (cover page).

(a) [15] Sketch v_O versus v_A for $v_B = 0$ and for $v_B = V_{DD}$ (two lines). What function does this circuit implement?

(b) [15] Calculate V_L and V_H and indicate on the plot in (a).

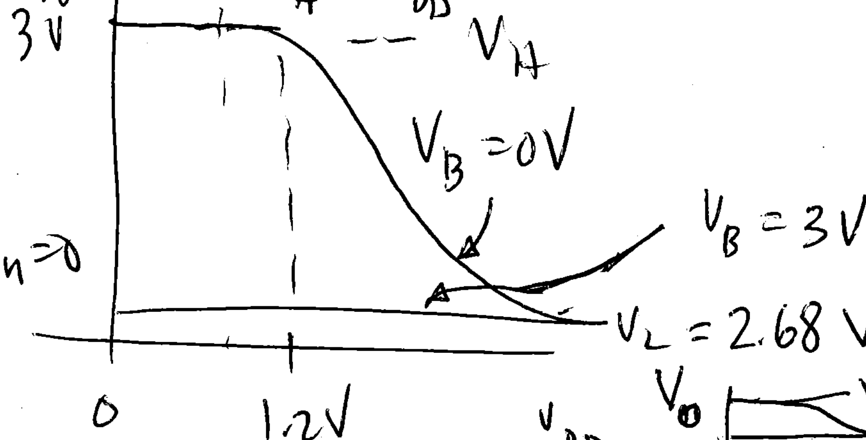


(a) $V_B = V_{DD} \Rightarrow D_B$ on $\Rightarrow V_{in} = V_{DD} - V_{on}$

$= 2.3\text{V}$

D_A off as long as $V_A \le V_{DD}$

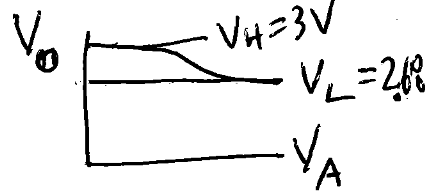
$V_o = V_L =$



$V_B = 0 \Rightarrow D_B$ off

$V_A \le V_{on}$, D_A off $\Rightarrow V_{in} = 0$

$V_A > V_{on}$ D_A on



$\Rightarrow V_{in} = V_A - V_{on} = V_A - 0.7\text{V}$

MOS turns on when $V_{in} > V_T = 0.5\text{V}$, so $V_A > 1.2\text{V}$

(b) $\frac{V_{DD} - V_L}{R_L} = \left(V_A - V_{on} - V_T - \frac{V_L}{2}\right) V_L \left(K_n' \frac{W}{L}\right)$ Assume linear

$V_H = 3\text{V}$ (MOS off)

$3\text{V} - V_L = \left(3\text{V} - 0.7\text{V} - 0.5\text{V} - \frac{V_L}{2}\right) V_L \underbrace{(0.2\,\text{V}^{-1})}_{K_n R_L}$ $200 \frac{\mu A}{V^2}$

$3\text{V} - V_L = (1.8\text{V})(0.2\text{V}^{-1}) V_L - 0.1 V_L^2$

$0.1 V_L^2 - 1.36 V_L + 3 = 0$ $\quad V_L = \frac{1.36 \pm \sqrt{(1.36)^2 - 1.2}}{0.2}$

$= 2.77$ V $\Rightarrow$ saturated

Redo

$\frac{3\text{V} - V_L}{R_L} = \frac{K_n}{2}(1.8\text{V})^2$

$3\text{V} - V_L = 0.1(1.8\text{V})^2$ $\quad V_L = 3\text{V} - 0.324\text{V} = 2.68\text{V}$

4. [34 points] Design a CMOS gate that implements the logic function $Z = \bar{A} + \bar{B} \cdot (C + \bar{D})$. Assume both inverted and noninverted logic signals are available.

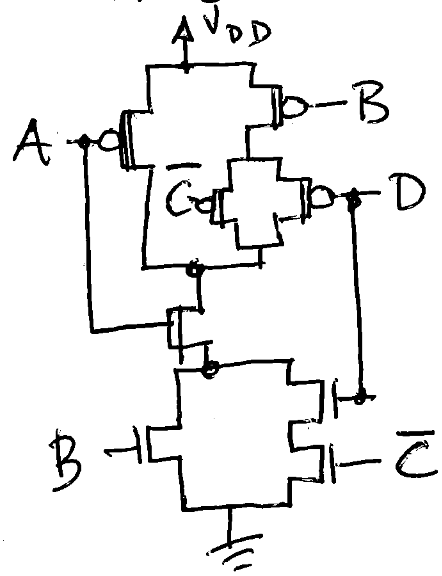
(a) [12] Draw the CMOS circuit design.

(b) [12] Design the aspect ratios for all transistors to make worst case VTC and switching speed equivalent to inverter with (W/L) for nMOS of (1/1) and (W/L) for pMOS of (2/1).

(c) [10] For your design, calculate the worst-case initial (just after input switches between V_H and V_L) pull-up current for V_{DD} = 1.5 V. Use γ = 0 (or α = 0.2 for 5 points bonus credit).

(a) $Z = \bar{A} + \bar{B}\cdot(C+\bar{D})$ is in pull-up (PMOS) form already

$$= \overline{A \cdot \overline{\bar{B}\cdot(C+\bar{D})}} = \overline{A \cdot (B + \overline{C+\bar{D}})} = \overline{A \cdot (B + (\bar{C} D))}$$



(b) $\left(\frac{W}{L}\right)^{A}_{PMOS} = \left(\frac{W}{L}\right)^{inverter}_{PMOS} = \frac{2}{1}$

$\left(\frac{W}{L}\right)^{B}_{PMOS} = \left(\frac{W}{L}\right)^{\bar{C}}_{PMOS} = \left(\frac{W}{L}\right)^{D}_{PMOS} = 2\left(\frac{W}{L}\right)^{inverter}_{PMOS} = 4/1$

as worst-case path has 2 PMOS

$\left(\frac{W}{L}\right)^{A}_{NMOS} = \left(\frac{W}{L}\right)^{B}_{NMOS} = 2\left(\frac{W}{L}\right)^{inverter}_{NMOS} = \frac{2}{1}$

$\left(\frac{W}{L}\right)^{\bar{C}}_{NMOS} = \left(\frac{W}{L}\right)^{D}_{NMOS} = 4\left(\frac{W}{L}\right)^{inverter}_{NMOS} = 4/1$

(c) $V_0 = V_L = 0V$ for CMOS

$V_I = V_L = 0V$ Can consider either ~~PMOS~~$_A$ on or $PMOS_B$ & $PMOS_D$

Easier to consider just $PMOS_A \Rightarrow V_{DS} = V_{DD} = 1.5V = V_{GS} \Rightarrow$ sat

$$I_{pull\text{-}up} = \frac{K_p'}{2}\left(\frac{W}{L}\right)_A (V_{DD} + V_{TP})^2 = \frac{100\mu A/V^2}{2}\left(\frac{2}{1}\right)(+1.5V - 0.5V)^2$$

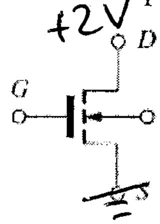
$$= 100\mu A \quad w/\ \gamma = 0\ (\alpha = 0)$$

With $\alpha = 0.2$ $\quad I_{pull\text{-}up} = \frac{100\mu A}{1+\alpha} = 83.3\mu A$

Note that if you consider series of B & D, $PMOS_B$ will be linear and $PMOS_D$ saturated. Result is same answer

5. [30 points] For problems below, use parameters on cover page, except assume $\gamma = 0$.

(a) [10] $V_S = 0$ V and $V_D = 2$ V. The current **into** terminal D is 2 mA. Find V_G. What mode is transistor operating in?



NMOS ~~transistor~~

Assume ~~saturated~~

$I_{DS} = 2mA = \frac{200\mu A/V^2}{2}(V_G - 0.5V)^2$

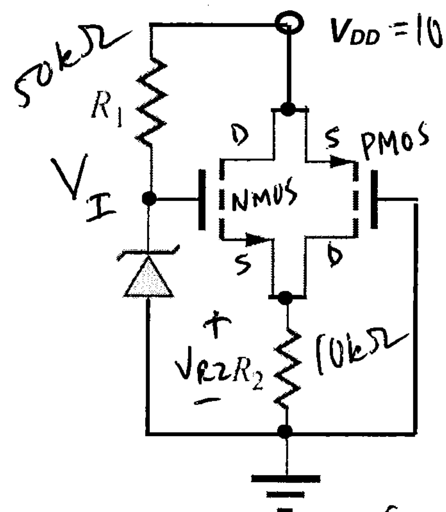
$\Rightarrow V_G = 4.97V \Rightarrow$ linear

$I_{DS} = 2mA = 200\mu A/V^2\left[V_G - 0.5V - \frac{2V}{2}\right]2V$

$10V^2/2V = 5V = V_G - 0.5V - 1V \Rightarrow \underline{V_G = 6.5V}$

Linear/triode mode

(b) [20] $V_{DD} = 10$ V, $R_1 = 50$ kΩ, and $R_2 = 10$ kΩ. $(W/L) = 1$ for both transistors. Determine the mode of each transistor and the voltage across resistor R_2.



$V_{DD} > V_{Zener}$, so $V_I = V_{Zener} = 5V$

$V_{GS}^{PMOS} = -10V$, Assume Linear ✓

Assume NMOS off ✓

$I_{SD} = K_p\left[10V - 0.5V - \frac{(10 - V_{R2})}{2}\right](10 - V_{R2})$

$= \frac{100\mu A}{V^2}\left[9.5 - 5 + \frac{V_{R2}}{2}\right](10 - V_{R2}) = \frac{V_{R2}}{10k\Omega}$

$(100\mu A)(10k\Omega) = 1V$

$1V^{-1}\left(4.5V + \frac{V_{R2}}{2}\right)(10V - V_{R2}) = V_{R2} \Rightarrow 45V + 0.5V_{R2} - \frac{V_{R2}^2}{2V} = V_{R2}$

$\frac{V_{R2}^2}{2} + 0.5V_{R2} - 45V = 0 \quad V_{R2}^2 + V_{R2} - 90V = 0$

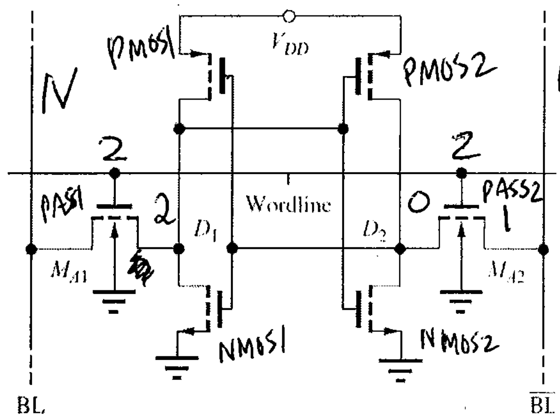
$\underline{V_{R2} = 9V}$ Check $\cancel{10^{-4}}\left(4.5 + \frac{9}{2}\right)(10 - 9) = \frac{9}{\cancel{10^4}}$ ✓

$V_{GS}^{NMOS} = 5V - 9V = -4V \Rightarrow OFF$

$V_{DS}^{PMOS} = 9V - 10V = -1V$ less negative than $V_{GS} - V_T = -10V + 0.5V = -9.5V$

$\Rightarrow$ triode/linear ✓

6. [30 points] In the SRAM cell to the right, $V_{DD} = 2$ V. Use MOS parameters on cover page, except use assume $\gamma = 0$. $\frac{W}{L} = 1$



(a) [15] $V_{D1} = 2$ V, $V_{D2} = 0$ V, and both bitlines are precharged to 1 V. What would be the initial current **into** each bit line (BL and $\overline{BL}$) immediately after the wordline voltage is switched from 0 to 2 V?

(b) [15] Initially, $V_{D1} = 2$ V and $V_{D2} = 0$ V. If the bit line voltages are held to $V_{BL} = 0$ V and $V_{\overline{BL}} = 0$ V and the wordline at 2 V, what is the final steady-state value for V_{D1} if V_{D2} remains near 0 V?

(a) For BL $V_G = 2V,\ V_S = 1V,\ V_D = 2V \Rightarrow V_{DS} = V_{GS} \Rightarrow$ saturated

$$I_{BL} = \frac{200\mu A/V^2}{2}(2V - 1V - 0.5V)^2 = \underline{+25\mu A}$$

For $\overline{BL}$ $V_G = 2V,\ V_S = 0V,\ V_D = 1V \Rightarrow V_{GS} > V_{DS} + V_T \Rightarrow$ linear

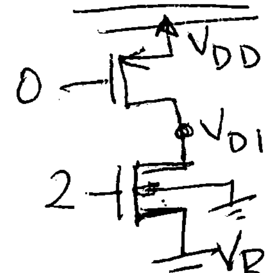
$$I_{\overline{BL}} = -I_{DS} = -200\mu A/V^2\left((2V - 0) - 0.5V - \frac{(1V - 0)}{2}\right)(1V - 0)$$

$$= -200\frac{\mu A}{V^2}(1V)(1V) = \underline{-200\mu A}$$

(b) $V_{D2} = V_{G1} = 0V$ $V_{BL} = 0V$

PMOS1 ON Pass Gate 1 ON

NMOS1 OFF



PMOS1

PASS1

$$K_p = K_p'\left(\frac{W}{L}\right)_p = 100\mu A/V^2(1) = 100\mu A/V^2$$

$$K_n = K_n'\left(\frac{W}{L}\right)_N = 200\mu A/V^2$$

Assume both transistors in linear/triode

$$\left(2V - 0.5V - \frac{(2 - V_{D1})}{2}\right)(2 - V_{D1}) = \frac{K_n}{K_p}\left(2V - 0.5V - \frac{V_{D1}}{2}\right)V_{D1}$$

$$\left(2 - 0.5 - 1 + \frac{V_{D1}}{2}\right)(2 - V_{D1}) = 2\left(1.5 - \frac{V_{D1}}{2}\right)V_{D1}$$ $V_{D1} = 0.44V$

$$\left(0.5 + \frac{V_{D1}}{2}\right)(2 - V_{D1}) = (3 - V_{D1})V_{D1}$$ $\Rightarrow V_{DS}^{PMOS} = -1.56V \Rightarrow$ Saturated

$$1 - \frac{V_{D1}}{2} + V_{D1} - \frac{V_{D1}^2}{2} = 3V_{D1} - V_{D1}^2 \Rightarrow \frac{V_{D1}^2}{2} - 2.5V_{D1} + 1 = 0$$

Redo w/ PMOS saturated

$$\frac{K_p}{2}(2-0.5)^2 = K_n\left(1.5 - \frac{V_{D1}}{2}\right)V_{D1}$$

$$(1.5)^2 = 4\left(1.5-\frac{V_{D1}}{2}\right)V_{D1} = 6V_{D1} - 2V_{D1}^2$$

$$2V_{D1}^2 - 6V_{D1} + 2.25 = 0$$

$$V_{D1} = \frac{6 \pm \sqrt{6^2-4(2.25)(2)}}{4} = \underline{0.44V}$$

Same answer since PMOS is barely saturated