PROBLEMS

Use the parameters in Table 4.6 as needed in the problems here.

TABLE 4.6
MOS Transistor Parameters

	NMOS DEVICE	PMOS DEVICE
V_{TO}	+0.75 V	−0.75 V
γ	$0.75\sqrt{\text{V}}$	$0.5\sqrt{\text{V}}$
$2\phi_F$	0.6 V	0.6 V
K′	100 μA/V²	40 μA/V²

$\varepsilon_{ox} = 3.9\varepsilon_o$ and $\varepsilon_s = 11.7\varepsilon_o$ where $\varepsilon_o = 8.854 \times 10^{-14}$ F/cm

4.1 Characteristics of the MOS Capacitor

4.1. (a) The MOS capacitor in Fig. 4.1 has $V_{TN} = 1$ V and $V_G = 2$ V. To what region of operation does this bias condition correspond? (b) Repeat for $V_G = -2$ V. (c) Repeat for $V_G = 0.5$ V.

4.2. Calculate the capacitance of an MOS capacitor with an oxide thickness T_{ox} of (a) 50 nm, (b) 25 nm, (c) 10 nm, and (d) 5 nm.

4.3. The minimum value of the depletion-layer capacitance can be estimated using an expression similar to Eq. (3.18): $C_d = \varepsilon_S / x_d$ in which the depletion-layer width is $x_d \cong \sqrt{\frac{2\varepsilon_S}{qN_B}(0.75\text{ V})}$ and N_B is the substrate doping. Estimate C_d for $N_B = 10^{-15}/\text{cm}^3$.

4.2 The NMOS Transistor

Triode (Linear) Region Characteristics

4.4. Calculate K_n' for an NMOS transistor with $\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$ for an oxide thickness of (a) 40 nm, (b) 20 nm, (c) 10 nm, and (d) 5 nm.

4.5. (a) What is the charge density (C/cm²) in the channel if the oxide thickness is 25 nm and the oxide voltage exceeds the threshold voltage by 1 V? (b) Repeat for a 10-nm oxide and a bias 1.5 V above threshold.

4.6. (a) What is the electron velocity in the channel if $\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$ and the electric field is 5000 V/cm? (b) Repeat for $\mu_n = 400\ \text{cm}^2/\text{V}\cdot\text{s}$ with a field of 2000 V/cm.

4.7. Equation (4.2) indicates that the charge/unit · length in the channel of a pinched-off transistor decreases as one proceeds from source to drain. However, our text argued that the current entering the drain terminal is equal to the current exiting from the source terminal. How can a constant current exist everywhere in the channel between the drain and source terminals if the first statement is indeed true?

4.8. An NMOS transistor has $K_n' = 200\ \mu\text{A/V}^2$. What is the value of K_n if $W = 60\ \mu$m, $L = 3\ \mu$m? If $W = 3\ \mu$m, $L = 0.15\ \mu$m? If $W = 10\ \mu$m, $L = 0.25\ \mu$m?

4.9. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 0.25$ V, if $W = 5\ \mu$m, $L = 0.5\ \mu$m, $V_{TN} = 0.80$ V, and $K_n' = 200\ \mu\text{A/V}^2$. What is the value of K_n?

4.10. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 0.1$ V, if $W = 10\ \mu$m, $L = 0.2\ \mu$m, $V_{TN} = 1.0$ V, and $K_n' = 250\ \mu\text{A/V}^2$. What is the value of K_n?

4.11. Identify the source, drain, gate, and bulk terminals and find the current I in the transistors in Fig. P4.11. Assume $V_{TN} = 0.70$ V.

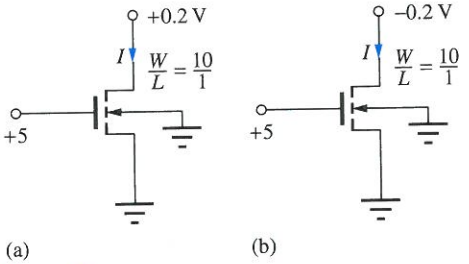

Figure P4.11

4.12. (a) What is the current in the transistor in Fig. P4.11(a) if the 0.2 V is changed to 0.5 V? Assume $V_{TN} = 0.70$ V. (b) Repeat if the gate voltage is changed to 3 V and the other voltage remains at 0.2 V?

4.13. (a) What is the current in the transistor in Fig. P4.11(b) if −0.2 V is changed to −0.5 V? Assume $V_{TN} = 0.75$ V. (b) If the gate voltage is changed to 3 V and the upper terminal voltage is replaced by −1 V?

4.14. (a) Design a transistor (choose W) to have $K_n = 4\ \text{mA/V}^2$ if $L = 0.5\ \mu$m. (See Table 4.6.) (b) Repeat for $K_n = 750\ \mu\text{A/V}^2$.

On Resistance

4.15. What is the on-resistance of an NMOS transistor with $W/L = 100/1$ if $V_{GS} = 5$ V and $V_{TN} = 0.65$ V? (b) If $V_{GS} = 2.5$ V and $V_{TN} = 0.50$ V? (See Table 4.6.)

4.16. (a) What is the W/L ratio required for an NMOS transistor to have an on-resistance of 500 Ω when $V_{GS} = 5$ V and $V_{SB} = 0$? (b) Repeat for $V_{GS} = 3.3$ V.

4.17. Suppose that an NMOS transistor must conduct a current $I_D = 10$ A with $V_{DS} \leq 0.1$ V when it is on. What is the maximum on-resistance of the transistor? If $V_G = 5$ V is used to turn on the transistor and $V_{TN} = 2$ V, what is the minimum value of K_n required to achieve the required on-resistance?

Saturation of the i-v Characteristics

*4.18. The output characteristics for an NMOS transistor are given in Fig. P4.18. What are the values of K_n and V_{TN} for this transistor? Is this an enhancement-mode or depletion-mode transistor? What is W/L for this device?

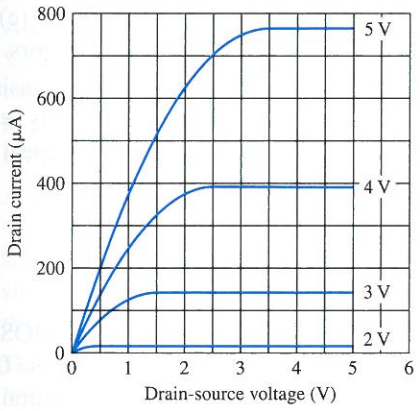

Figure P4.18

4.19. Add the $V_{GS} = 3.5$ V and $V_{GS} = 4.5$ V curves to the i-v characteristic of Fig. P4.18. What are the values of i_{DSAT} and v_{DSAT} for these new curves?

4.20. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 3.3$ V, if $W = 5$ μm, $L = 0.5$ μm, $V_{TN} = 1$ V, and $K'_n = 375$ μA/V^2. What is the value of K_n? Check the saturation region assumption.

4.21. Calculate the drain current in an NMOS transistor for $V_{GS} = 0$, 1 V, 2 V, and 3 V, with $V_{DS} = 4$ V, if $W = 10$ μm, $L = 1$ μm, $V_{TN} = 1.5$ V, and $K'_N = 200$ μA/V^2. What is the value of K_n? Check the saturation region assumption.

Regions of Operation

4.22. Find the region of operation and drain current in an NMOS transistor with $K'_n = 200$μA/V^2, $W/L = 10/1$, $V_{TN} = 0.75$ V and (a) $V_{GS} = 2$ V and $V_{DS} = 2.5$ V, (b) $V_{GS} = 2$ V and $V_{DS} = 0.2$ V, (c) $V_{GS} = 0$ V and $V_{DS} = 4$ V. (d) Repeat for $K'_n = 300$μA/V^2.

4.23. Identify the region of operation of an NMOS transistor with $K_n = 400$ μA/V^2 and $V_{TN} = 0.7$ V for (a) $V_{GS} = 3.3$ V and $V_{DS} = 3.3$ V, (b) $V_{GS} = 0$ V and $V_{DS} = 3.3$ V, (c) $V_{GS} = 2$ V and $V_{DS} = 2$ V, (d) $V_{GS} = 1.5$ V and $V_{DS} = 0.5$, (e) $V_{GS} = 2$ V and $V_{DS} = -0.5$ V, and (f) $V_{GS} = 3$ V and $V_{DS} = -3$ V.

4.24. Identify the region of operation of an NMOS transistor with $K_n = 250$ μA/V^2 and $V_{TN} = 1$ V for (a) $V_{GS} = 5$ V and $V_{DS} = 6$ V, (b) $V_{GS} = 0$ V and $V_{DS} = 6$ V, (c) $V_{GS} = 2$ V and $V_{DS} = 2$ V, (d) $V_{GS} = 1.5$ V and $V_{DS} = 0.5$, (e) $V_{GS} = 2$ V and $V_{DS} = -0.5$ V, and (f) $V_{GS} = 3$ V and $V_{DS} = -6$ V.

4.25. (a) Identify the source, drain, gate, and bulk terminals for the transistor in the circuit in Fig. P4.25. Assume $V_{DD} > 0$. (b) Repeat for $V_{DD} < 0$. (c) An issue occurs with operation of the circuit in Fig. P4.25 with $V_{DD} < 0$. What is the problem?

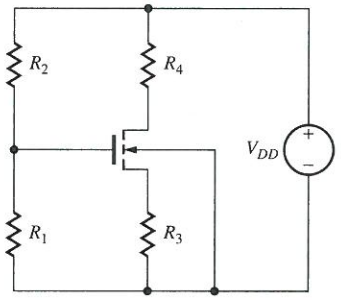

Figure P4.25

4.26. (a) Identify the source, drain, gate, and bulk terminals for each of the transistors in the circuit in Fig. P4.26(a). Assume $V_{DD} > 0$. (b) Repeat for the circuit in Fig. P4.26(b).

Transconductance

4.27. Calculate the transconductance for an NMOS transistor for $V_{GS} = 2$ V and 3.3 V, with $V_{DS} = 3.3$ V, if $W = 20$ μm, $L = 1$ μm, $V_{TN} = 0.7$ V, and $K'_n = 250$ μA/V^2. Check the saturation region assumption.

4.28. (a) Estimate the transconductance for the transistor in Fig. P4.18 for $V_{GS} = 4$ V and $V_{DS} = 4$ V.

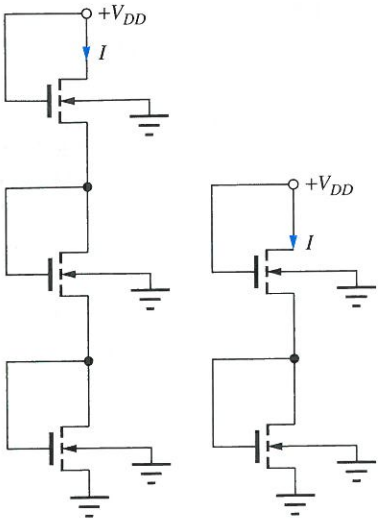

Figure P4.26

(*Hint:* $g_m \cong \Delta i_D / \Delta V_{GS}$.) (b) Repeat for $V_{GS} = 3$ V and $V_{DS} = 4.5$ V.

4.29. Find an expression for the transconductance of the MOSFET in the linear region. What is the transconductance of the MOSFET in Prob. 4.27 with $V_{GS} = 2$ V and 3.3 V with $V_{DS} = 1$ V?

Channel-Length Modulation

4.30. (a) Calculate the drain current in an NMOS transistor if $K_n = 500\ \mu\text{A/V}^2$, $V_{TN} = 1$ V, $\lambda = 0.02\ \text{V}^{-1}$, $V_{GS} = 4$ V, and $V_{DS} = 5$ V. (b) Repeat assuming $\lambda = 0$.

4.31. (a) Calculate the drain current in an NMOS transistor if $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = 0.75$ V, $\lambda = 0.025\ \text{V}^{-1}$, $V_{GS} = 5$ V, and $V_{DS} = 6$ V. (b) Repeat assuming $\lambda = 0$.

4.32. (a) Find the drain current for the transistor in Fig. P4.32 if $\lambda = 0$. (b) Repeat if $\lambda = 0.025\ \text{V}^{-1}$. (c) Repeat part (a) if the W/L ratio is changed to 25/1.

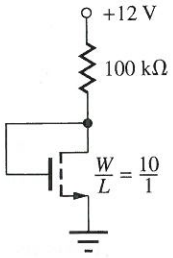

Figure P4.32

4.33. (a) Find the drain current for the transistor in Fig. P4.32 if $\lambda = 0$ and the W/L ratio is changed to 20/1. (b) Repeat if $\lambda = 0.020\ \text{V}^{-1}$.

4.34. (a) Find the current I in Fig. P4.34 if $V_{DD} = 10$ V and $\lambda = 0$. Both transistors have $W/L = 10/1$. (b) What is the current if both transistors have $W/L = 20/1$. (c) Repeat part (a) for $\lambda = 0.04\ \text{V}^{-1}$.

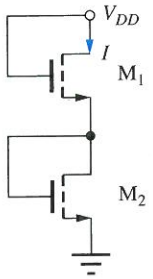

Figure P4.34

4.35. (a) Find the currents in the two transistors in Fig. P4.34 if $(W/L)_1 = 10/1$, $(W/L)_2 = 40/1$, and $\lambda = 0$ for both transistors. (b) Repeat for $(W/L)_2 = 40/1$ and $(W/L)_1 = 10/1$. (c) Repeat part (a) if $\lambda = 0.05$/V for both transistors.

4.36. (a) Find the currents in the two transistors in Fig. P4.34 if $(W/L)_1 = 25/1$, $(W/L)_2 = 12.5/1$ and $\lambda = 0$ for both transistors. (b) Repeat part (a) if $\lambda = 0.05$/V for both transistors.

Transfer Characteristics and the Depletion-Mode MOSFET

4.37. (a) Calculate the drain current in an NMOS transistor if $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = -3$ V, $\lambda = 0$, $V_{GS} = 0$ V, and $V_{DS} = 6$ V. (b) Repeat assuming $\lambda = 0.025\ \text{V}^{-1}$.

4.38. (a) Calculate the drain current in an NMOS transistor if $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = -2$ V, $\lambda = 0$, $V_{GS} = 5$ V, and $V_{DS} = 6$ V. (b) Repeat assuming $\lambda = 0.03\ \text{V}^{-1}$.

4.39. An NMOS depletion-mode transistor is operating with $V_{DS} = V_{GS} > 0$. What is the region of operation for this device?

4.40. (a) Find the Q-point for the transistor in Fig. P4.40(a) if $V_{TN} = -2$ V. (b) Repeat for $R = 50\ \text{k}\Omega$ and $W/L = 20/1$. (c) Repeat parts (a) & (b) for Fig. 4.40(b).

4.41. (a) Find the Q-point for the transistor in Fig. P4.40(a) if $V_{TN} = -1$ V and W/L is changed to 20/1. (b) Repeat for Fig. P4.40(b).

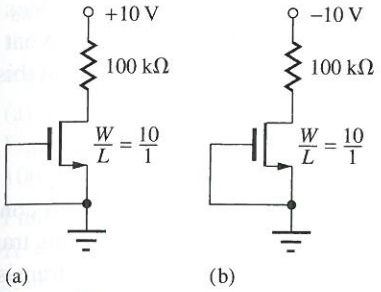

Figure P4.40

Body Effect or Substrate Sensitivity

4.42. Repeat Problem 4.20 with for $V_{SB} = 1.25$ V with the values from Table 4.6.

4.43. Repeat Prob. 4.21 for $V_{SB} = 1.5$ V with the values from Table 4.6.

4.44. (a) An NMOS transistor with $W/L = 8/1$ has $V_{TO} = 1$ V, $2\phi_F = 0.6$ V, and $\gamma = 0.7\sqrt{\text{V}}$. The transistor is operating with $V_{SB} = 3$ V, $V_{GS} = 2.5$ V, and $V_{DS} = 5$ V. What is the drain current in the transistor? (b) Repeat for $V_{DS} = 0.5$ V.

4.45. An NMOS transistor with $W/L = 16.8/1$ has $V_{TO} = 1.5$ V, $2\phi_F = 0.75$ V, and $\gamma = 0.5\sqrt{\text{V}}$. The transistor is operating with $V_{SB} = 4$ V, $V_{GS} = 2$ V, and $V_{DS} = 5$ V. What is the drain current in the transistor? (b) Repeat for $V_{DS} = 0.5$ V.

4.46. A depletion-mode NMOS transistor has $V_{TO} = -1.5$ V, $2\phi_F = 0.75$ V, and $\gamma = 1.5\sqrt{\text{V}}$. What source-bulk voltage is required to change this transistor into an enhancement-mode device with a threshold voltage of +0.85 V?

*4.47. The measured body-effect characteristic for an NMOS transistor is given in Table 4.7. What are the best values of V_{TO}, γ, and $2\phi_F$ (in the least-squares sense — see Prob. 3.30) for this transistor?

TABLE 4.7

V_{SB} (V)	V_{TN} (V)
0	0.710
0.5	0.912
1.0	1.092
1.5	1.232
2.0	1.377
2.5	1.506
3.0	1.604
3.5	1.724
4.0	1.822
4.5	1.904
5.0	2.005

4.3 PMOS Transistors

4.48. Calculate K'_p for a PMOS transistor with $\mu_p = 200$ cm^2/V · s for an oxide thickness of (a) 50 nm, (b) 20 nm, (c) 10 nm, and (d) 5 nm.

*4.49. The output characteristics for a PMOS transistor are given in Fig. P4.49. What are the values of K_p and V_{TP} for this transistor? Is this an enhancement-mode or depletion-mode transistor? What is the value of W/L for this device?

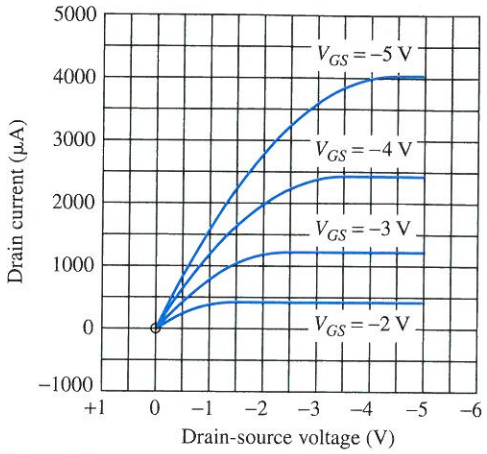

Figure P4.49

4.50. Add the $V_{GS} = -3.5$ V and $V_{GS} = -4.5$ V curves to the i-v characteristic of Fig. P4.49. What are the values of i_{DSAT} and v_{DSAT} for these new curves?

4.51. Find the region of operation and drain current in a PMOS transistor with $W/L = 20/1$ for $V_{BS} = 0$ V and (a) $V_{GS} = -1.1$ V and $V_{DS} = -0.2$ V and (b) $V_{GS} = -1.3$ V and $V_{DS} = -0.2$ V. (c) Repeat parts (a) and (b) for $V_{BS} = 1$ V.

4.52. (a) What is the W/L ratio required for an PMOS transistor to have an on-resistance of 2 kΩ when $V_{GS} = -5$ V and $V_{BS} = 0$? Assume $V_{TP} = -0.70$ V. (b) Repeat for an NMOS transistor with $V_{GS} = +5$ V and $V_{BS} = 0$. Assume $V_{TN} = 0.70$ V.

4.53. (a) What is the W/L ratio required for a PMOS transistor to have an on-resistance of 1 Ω when $V_{GS} = -5$ V and $V_{SB} = 0$? Assume $V_{TP} = -0.70$ V. (b) Repeat for an NMOS transistor with $V_{GS} = +5$ V and $V_{BS} = 0$. Assume $V_{TN} = 0.70$ V.

4.54. (a) Calculate the on-resistance for a PMOS transistor having $W/L = 200/1$ and operating with $V_{GS} = -5$ V and $V_{TP} = -0.75$ V. (b) Repeat for

a similar NMOS transistor with $V_{GS} = 5$ V and $V_{TN} = 0.75$ V. (c) What W/L ratio is required for the PMOS transistor to have the same R_{on} as the NMOS transistor in (b)?

4.55. (a) Identify the source, drain, gate, and bulk terminals for the transistors in the two circuits in Fig. P4.55(a). Assume $V_{DD} = 10$ V. (b) Repeat for Fig. P4.55(b).

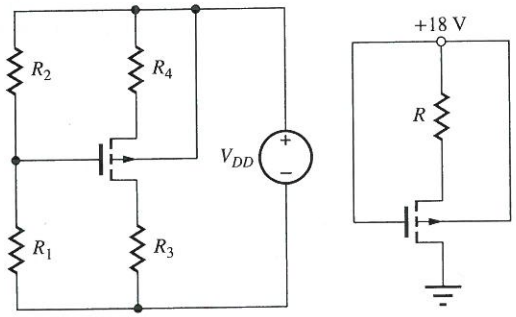

Figure P4.55

4.56. What is the on-resistance and voltage V_O for the parallel combination of the NMOS ($W/L = 10/1$) and PMOS ($W/L = 25/1$) transistors in Fig. P4.56 for $V_{IN} = 0$ V? (b) For $V_{IN} = 5$ V? This circuit is called a transmission-gate.

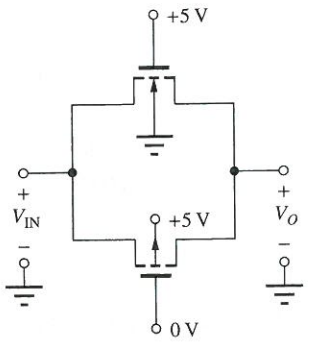

Figure P4.56

4.57. Suppose a PMOS transistor must conduct a current $I_D = 0.5$ A with $V_{SD} \leq 0.1$ V when it is on. What is the maximum on-resistance? If $V_G = 0$ V is used to turn on the transistor with $V_S = 10$ V and $V_{TP} = -2$ V, what is the minimum value of K_p required to achieve the required on-resistance?

4.58. A PMOS transistor is operating with $V_{BS} = 0$ V, $V_{GS} = -1.5$ V, and $V_{DS} = -0.5$ V. What are the region of operation and drain current in this device if $W/L = 40/1$?

4.59. A PMOS transistor is operating with $V_{BS} = 4$ V, $V_{GS} = -1.5$ V, and $V_{DS} = -4$ V. What are the region of operation and drain current in this device if $W/L = 25/1$?

4.4 MOSFET Circuit Symbols

4.60. The PMOS transistor in Fig. P4.55(a) is conducting current. Is $V_{TP} > 0$ or $V_{TP} < 0$ for this transistor? Based on this value of V_{TP}, what type transistor is in the circuit? Is the proper symbol used in this circuit for this transistor? If not, what symbol should be used?

4.61. The PMOS transistor in Fig. P4.55(b) is conducting current. Is $V_{TP} > 0$ or $V_{TP} < 0$ for this transistor? Based on this value of V_{TP}, what type transistor is in the circuit? Is the proper symbol used in this circuit for this transistor? If not, what symbol should be used?

4.62. (a) Redraw the circuits in Fig. P4.55(a) with a three-terminal PMOS transistor with its body connected to its source. (b) Repeat for Fig. P4.55(b).

4.63. Redraw the circuit in Fig. 4.27 with a four-terminal NMOS transistor with its body connected to -3 V.

4.64. Redraw the circuit in Fig. 4.28 with a four-terminal NMOS transistor with its body connected to -5 V.

4.5 Capacitances in MOS Transistors

4.65. Calculate C''_{ox} and C_{GC} for an MOS transistor with $W = 10$ μm and $L = 0.25$ μm with an oxide thickness of (a) 50 nm, (b) 20 nm, (c) 10 nm, and (d) 5nm.

4.66. Calculate C''_{ox} and C_{GC} for an MOS transistor with $W = 5$ μm and $L = 0.5$ μm with an oxide thickness of (a) 25 nm and (b) 10 nm.

4.67. In a certain MOSFET, the value of C'_{OL} can be calculated using an effective overlap distance of 0.5 μm. What is the value of C'_{OL} for an oxide thickness of 10 nm.

4.68. What are the values of C_{GS} and C_{GD} for a transistor with $C''_{ox} = 1.4 \times 10^{-3}$ F/m^2 and $C'_{OL} = 5 \times 10^{-9}$ F/m if $W = 10$ μm and $L = 1$ μm operating in (a) the triode region, (b) the saturation region, and (c) cutoff?

4.69. A large-power MOSFET has an effective gate area of 60×10^6 μm^2. What is the value of C_{GC} if T_{ox} is 100 nm?

4.70. (a) Find C_{GS} and C_{GD} for the transistor in Fig. 4.22 for the triode region if $\Lambda = 0.5$ μm, $T_{ox} = 150$ nm,

and $C_{GSO} = C_{GDO} = 20$ pF/m. (b) Repeat for the saturation region. (c) Repeat for the cutoff region.

4.71. (a) Repeat Prob. 4.70 for a transistor similar to Fig. 4.22 but with $W/L = 10/1$. (b) With $W/L = 100/1$. Assume $L = 1$ μm.

4.72. Find C_{SB} and C_{DB} for the transistor in Fig. 4.22 if $\Lambda = 0.5$ μm, the substrate doping is $10^{16}/\text{cm}^3$, the source and drain doping is $10^{20}/\text{cm}^3$, and $C_{JSW} = C_J \times (5 \times 10^{-4}\,/\text{cm})$.

4.6 MOSFET Modeling in SPICE

4.73. What are the values of SPICE model parameters KP, LAMBDA, VTO, PHI, W, and L for a transistor with the following characteristics: $V_{TN} = 0.7$ V, $K_n = 175\ \mu\text{A/V}^2$, $W = 5$ μm, $L = 0.25$ μm, $\lambda = 0.02\ \text{V}^{-1}$, and $2\phi_F = 0.8$ V?

4.74. What are the values of SPICE model parameters KP, LAMBDA, VTO, W and L for the transistor in Fig. 4.7 if $K_n' = 50\ \mu\text{A/V}^2$ and $L = 0.5$ μm?

4.75. What are the values of SPICE model parameters KP, LAMBDA, VTO, W and L for the transistor in Fig. 4.8 if $K_n' = 10\ \mu\text{A/V}^2$ and $L = 0.6$ μm?

4.76. (a) What are the values of SPICE model parameters VTO, PHI, and GAMMA for the transistor in Fig. 4.13? (b) Repeat for the transistor in Prob. 4.45.

4.77. What are the values of SPICE model parameters KP, LAMBDA, VTO, W and L, for the transistor in Fig. 4.14 if $K_p' = 10\ \mu\text{A/V}^2$ and $L = 0.5$ μm?

4.78. What are the values of SPICE model parameters KP, LAMBDA, VTO, W and L, for the transistor in Fig. 4.24(b) if $K_n' = 25\ \mu\text{A/V}^2$ and $L = 0.6$ μm?

4.7 MOS Transistor Scaling

4.79. (a) A transistor has $T_{ox} = 40$ nm, $V_{TN} = 1$ V, $\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$, $L = 2$ μm, and $W = 20$ μm. What are K_n and the saturated value of i_D for this transistor if $V_{GS} = 4$ V? (b) The technology is scaled by a factor of 2. What are the new values of T_{ox}, W, L, V_{TN}, V_{GS}, K_n, and i_D?

4.80. (a) A transistor has an oxide thickness of 20 nm with $L = 1$ μm and $W = 20$ μm. What is C_{GC} for this transistor? (b) The technology is scaled by a factor of 2. What are the new values of T_{ox}, W, L, and C_{GC}?

4.81. Show that the cutoff frequency of a PMOS device is given by $f_T = \frac{1}{2\pi}\frac{\mu_p}{L^2}|V_{GS} - V_{TP}|$.

4.82. (a) An NMOS device has $\mu_n = 400\ \text{cm}^2/\text{V}\cdot\text{s}$. What is the cutoff frequency for $L = 1$ μm if the transistor is biased at 1 V above threshold? What would be the cutoff frequency of a similar PMOS device if $\mu_p = 0.4\ \mu_n$? (b) Repeat for $L = 0.1$ μm.

4.83. An NMOS transistor has $T_{ox} = 80$ nm, $\mu_n = 400\ \text{cm}^2/\text{V}\cdot\text{s}$, $L = 0.1$ μm, $W = 2$ μm, and $V_{GS} - V_{TN} = 2$ V. (a) What is the saturation region current predicted by Eq. (4.17)? (b) What is the saturation current predicted by Eq. (4.49) if we assume $v_{SAT} = 10^7$ cm/s?

4.84. The NMOS transistor in Fig. 4.19 is biased with $V_{GS} = 0$ V. What is the drain current? (b) What is the drain current if the threshold voltage is reduced to 0.5 V?

4.8 MOS Transistor Fabrication and Layout Design Rules

4.85. Layout a transistor with $W/L = 10/1$ similar to Fig. 4.22. What fraction of the total area does the channel represent?

4.86. Layout a transistor with $W/L = 5/1$ similar to Fig. 4.22 using $T = F = 2\,\Lambda$. What fraction of the total area does the channel represent?

4.87. Layout a transistor with $W/L = 5/1$ similar to Fig. 4.22 but change the alignment so that masks 2, 3, and 4 are all aligned to mask 1. What fraction of the total area does the channel represent?

4.88. Layout a transistor with $W/L = 5/1$ similar to Fig. 4.22 but change the alignment so that mask 3 is aligned to mask 1. What fraction of the total area does the channel represent?

4.9 Biasing the NMOS Field-Effect Transistor

Load Line Analysis

4.89. Draw the load line for the circuit in Fig. P4.89 on the output characteristics in Fig. P4.18 and locate the Q-point. Assume $V_{DD} = +4$ V. What is the operating region of the transistor?

4.90. Draw the load line for the circuit in Fig. P4.89 on the output characteristics in Fig. P4.18 and locate the Q-point. Assume $V_{DD} = +5$ V and the resistor is changed to 8.3 kΩ. What is the operating region of the transistor?

4.91. Draw the load line for the circuit in Fig. P4.91 on the output characteristics in Fig. P4.18 and locate the Q-point. Assume $V_{DD} = +6$ V. What is the operating region of the transistor?

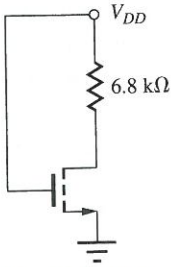

Figure P4.89

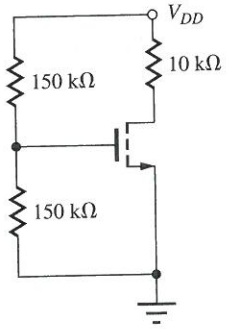

Figure P4.91

4.92. Draw the load line for the circuit in Fig. P4.91 on the output characteristics in Fig. P4.18 and locate the Q-point. Assume $V_{DD} = +8$ V. What is the operating region of the transistor?

Four-Resistor Biasing

4.93. (a) Find the Q-point for the transistor in Fig. P4.93 for $R_1 = 100$ kΩ, $R_2 = 220$ kΩ, $R_3 = 24$ kΩ, $R_4 = 12$ kΩ, and $V_{DD} = 10$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0$, and $W/L = 6/1$. (b) Repeat for $W/L = 12/1$.

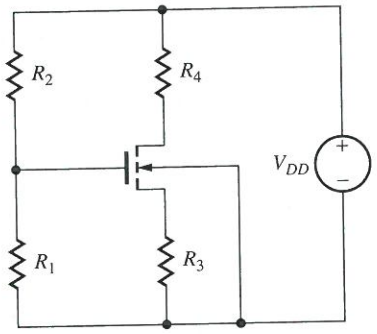

Figure P4.93

4.94. Repeat Prob. 4.93(a) if all resistor values are increased by a factor of 10.

4.95. Repeat Prob. 4.93(a) if all resistor values are reduced by a factor of 10 and $W/L = 20/1$. (b) Repeat for $W/L = 60/1$.

4.96. Repeat Prob. 4.93 with $V_{DD} = 12$ V.

4.97. Find the Q-point for the transistor in Fig. P4.93 for $R_1 = 200$ kΩ, $R_2 = 430$ kΩ, $R_3 = 47$ kΩ, $R_4 = 24$ kΩ, and $V_{DD} = 12$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0$, and $W/L = 5/1$. (b) Repeat for $W/L = 15/1$.

4.98. Use SPICE to simulate the circuit in Prob. 4.93 and compare the results to hand calculations.

4.99. Use SPICE to simulate the circuit in Prob. 4.96 and compare the results to hand calculations.

4.100. Use SPICE to simulate the circuit in Prob. 4.97 and compare the results to hand calculations.

4.101. The drain current in the circuit in Fig. 4.25 was found to be 50 μA. The gate bias circuit in the example could have been designed with many different choices for resistors R_1 and R_2. Some possibilities for (R_1, R_2) are (3 kΩ, 7 kΩ), (12 kΩ, 28 kΩ), (300 kΩ, 700 kΩ), and (1.2 MΩ, 2.8 MΩ). Which of these choices would be the best and why?

*4.102. Suppose the design of Ex. 4.4 is implemented with $V_{EQ} = 4$ V, $R_S = 1.7$ kΩ, and $R_D = 38.3$ kΩ. (a) What would be the Q-point if $K_n = 35$ μA/V^2? (b) If $K_n = 25$ μA/V^2 but $V_{TN} = 0.75$ V?

4.103. (a) Simulate the circuit in Ex. 4.3 and compare the results to the calculations. (b) Repeat for the circuit design in Ex. 4.4.

4.104. Design a four-resistor bias network for an NMOS transistor to give a Q-point of (500 μA, 5 V) with $V_{DD} = 15$ V and $R_{EQ} \cong 600$ kΩ. Use the parameters from Table 4.6.

4.105. Design a four-resistor bias network for an NMOS transistor to give a Q-point of (250 μA, 3 V) with $V_{DD} = 9$ V and $R_{EQ} \cong 250$ kΩ. Use the parameters from Table 4.6.

4.106. Design a four-resistor bias network for an NMOS transistor to give a Q-point of (100 μA, 4 V) with $V_{DD} = 12$ V and $R_{EQ} \cong 250$ kΩ. Use the parameters from Table 4.6.

Depletion-Mode Devices

4.107. What is the Q-point of the transistor in Fig. P4.93 if $R_1 = 470$ kΩ, $R_2 = \infty$, $R_3 = 27$ kΩ, $R_4 = 51$ kΩ, and $V_{DD} = 12$ V for $V_{TN} = -4$ V and $K_n = 600$ μA/V^2.

4.108. What is the Q-point of the transistor in Fig. P4.93 if $R_1 = 1$ MΩ, $R_2 = \infty$, $R_3 = 10$ kΩ, $R_4 = 5$ kΩ, and $V_{DD} = 15$ V for $V_{TN} = -5$ V and $K_n = 1$ mA/V^2.

*4.109. Design a bias network for a depletion-mode NMOS transistor to give a Q-point of (2 mA, 5 V) with $V_{DD} = 15$ V if $V_{TN} = -2.5$ V and $K_n = 250$ μA/V^2. (*Hint:* You may wish to consider the four-resistor bias network.)

4.110. Design a bias network for a depletion-mode NMOS transistor to give a Q-point of (250 μA, 5 V) with $V_{DD} = 15$ V if $V_{TN} = -4$ V and $K_n = 1$ mA/V^2.

Two-Resistor Biasing

The two-resistor bias circuit represents a simple alternative strategy for biasing the MOS transistor.

4.111. (a) Find the Q-point for the transistor in the circuit in Fig. P4.111(a) if $V_{DD} = +12$ V. (b) Repeat for the circuit in Fig. P4.111(b).

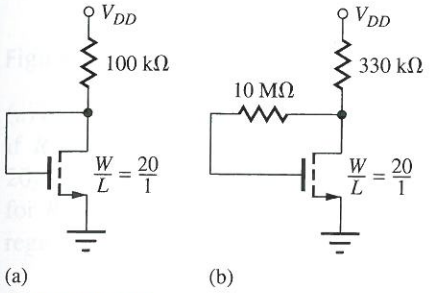

Figure P4.111

4.112. (a) Find the Q-point for the transistor in the circuit in Fig. P4.111(a) if $V_{DD} = +12$ V and W/L is changed to 101? (b) Repeat for the circuit in Fig. P4.111(b).

4.113. (a) Find the Q-point for the transistor in the circuit in Fig. P4.111(b) if $V_{DD} = +15$ V. (b) Repeat for $V_{DD} = +15$ V with W/L is changed to 25/1?

4.114. (a) Find the Q-point for the transistor in the circuit in Fig. P4.111(b) if $V_{DD} = +12$ V and the 330 kΩ resistor is increased to 470 kΩ. (b) Repeat if the 10 MΩ resistor is reduced to 2 MΩ.

Body Effect

4.115. Find the solution to Eq. set (4.58) using MATLAB. (b) Repeat for $\gamma = 0.75\ \sqrt{\text{V}}$.

4.116. Find the solution to Eq. set (4.58) using a spreadsheet if $\gamma = 0.75\ \sqrt{\text{V}}$. (b) Repeat for $\gamma = 1.25\ \sqrt{\text{V}}$.

4.117. Redesign the values of R_S and R_D in the circuit in Ex. 4.4 to compensate for the body effect and restore the Q-point to its original value (100 μA, 6 V).

4.118. Find the Q-point for the transistor in Fig. P4.93 for $R_1 = 100$ kΩ, $R_2 = 220$ kΩ, $R_3 = 24$ kΩ, $R_4 = 12$ kΩ, and $V_{DD} = 12$ V. Assume that $V_{TO} = 1$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, and $W/L = 5/1$.

*4.119. (a) Repeat Prob. 4.118 with $\gamma = 0.75\ \sqrt{\text{V}}$. (b) Repeat Prob. 4.118 with $R_4 = 24$ kΩ.

4.120. (a) Use SPICE to simulate the circuit in Prob. 4.118 and compare the results to hand calculations. (b) Repeat for Prob. 4.119(a). (c) Repeat for Prob. 4.119(b).

4.121. Simulate the circuit in Prob. 4.93 using (a) $\gamma = 0$ and (b) $\gamma = 0.5\ \text{V}^{-0.5}$ and $2\phi_F = 0.6$ V and compare the results. Does our neglect of body effect in hand calculations appear to be justified?

4.122. Simulate the circuit in Prob. 4.94 using (a) $\gamma = 0$ and (b) $\gamma = 0.5\ \text{V}^{-0.5}$ and $2\phi_F = 0.6$ V and compare the results. Does our neglect of body effect in hand calculations appear to be justified?

4.123. Simulate the circuit in Prob. 4.95 using (a) $\gamma = 0$ and (b) $\gamma = 0.5\ \text{V}^{-0.5}$ and $2\phi_F = 0.6$ V and compare the results. Does our neglect of body effect in hand calculations appear to be justified?

4.124. Simulate the circuit in Prob. 4.96 using (a) $\gamma = 0$ and (b) $\gamma = 0.5\ \text{V}^{-0.5}$ and $2\phi_F = 0.6$ V and compare the results. Does our neglect of body effect in hand calculations appear to be justified?

General Bias Problems

4.125. (a) Find the current I in Fig. P4.125 if $V_{DD} = 5$ V assuming that $\gamma = 0$, $V_{TO} = 1$ V, and the transistors both have $W/L = 20/1$. (b) Repeat for $V_{DD} = 10$ V. *(c) Repeat part (a) with $\gamma = 0.5\sqrt{\text{V}}$.

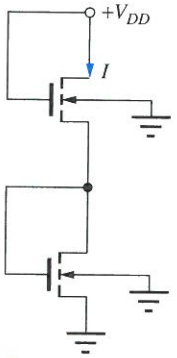

Figure P4.125

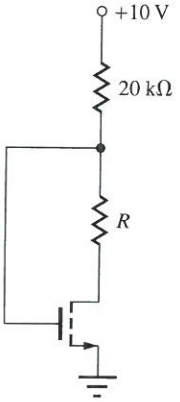

Figure P4.127

4.126. Find the Q-point for the transistor in Fig. P4.127 if $R = 10$ kΩ, $V_{TO} = 1$ V, and $W/L = 4/1$.

4.127. Find the Q-point for the transistor in Fig. P4.127 if $R = 20$ kΩ, $V_{TO} = 1$ V, and $W/L = 2/1$.

**4.128. (a) Find the current I in Fig. P4.128 assuming that $\gamma = 0$ and $W/L = 20/1$ for each transistor. (b) Repeat part (a) for $W/L = 50/1$. **(c) Repeat part (a) with $\gamma = 0.5\ \sqrt{\text{V}}$.

4.129. (a) Simulate the circuit in Fig. P4.128 using SPICE and compare the results to those of Prob. 4.128(a).

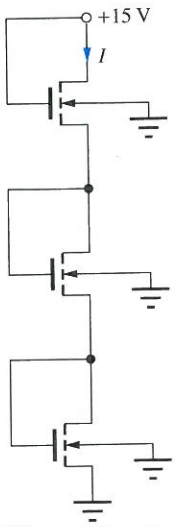

Figure P4.128

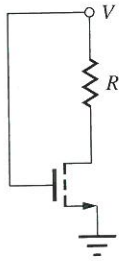

Figure P4.130

(b) Repeat for Prob. 4.128(b). **(c) Repeat for Prob. 4.128(c).

4.130. What value of W/L is required to set $V_{DS} = 0.50$ V in the circuit in Fig. P4.130 if $V = 5$ V and $R = 68$ kΩ?

4.131. What value of W/L is required to set $V_{DS} = 0.25$ V in the circuit in Fig. P4.130 if $V = 3.3$ V and $R = 160$ kΩ?

4.10 Biasing the PMOS Field-Effect Transistor

4.132. (a) Find the Q-point for the transistor in Fig. P4.132(a) if $V_{DD} = -15$ V, $R = 75$ kΩ, and $W/L = 1/1$. (b) Find the Q-point for the transistor in Fig. P4.132(b) if $V_{DD} = -15$ V, $R = 75$ kΩ, and $W/L = 1/1$.

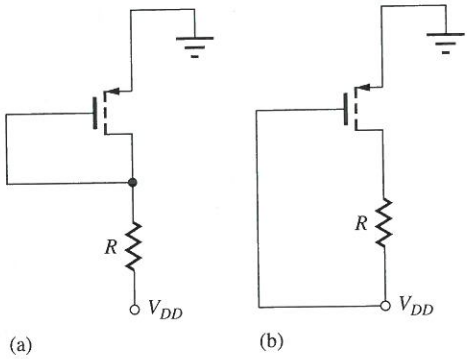

Figure P4.132

4.133. Simulate the circuits in Prob. 4.132 with $V_{DD} = -15$ V and compare the Q-point results to hand calculations.

*4.134. (a) Find current I and voltage V_O in Fig. P4.134(a) if $W/L = 20/1$ for both transistors and $V_{DD} = 10$ V. (b) What is the current if $W/L = 80/1$? (c) Repeat for the circuit in Fig. P4.134(b).

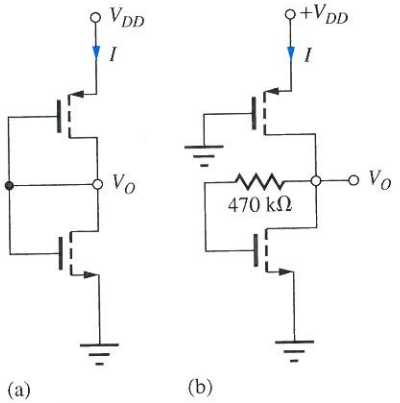

Figure P4.134

**4.135. (a) Find the current I in Fig. P4.135 assuming that $\gamma = 0$ and $W/L = 40/1$ for each transistor. (b) Repeat part (a) for $W/L = 75/1$. **(c) Repeat part (a) with $\gamma = 0.5\ \sqrt{\text{V}}$.

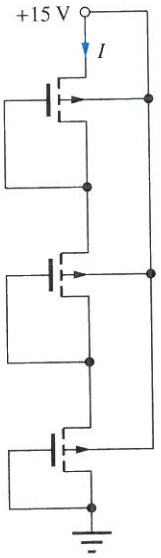

Figure P4.135

*4.136. (a) Simulate the circuit in Prob. 4.135(a) and compare the results to those of Prob. 4.135(a). (b) Repeat for Prob. 4.135(b). (c) Repeat for Prob. 4.135(c).

4.137. Draw the load line for the circuit in Fig. P4.137 on the output characteristics in Fig. P4.49 and locate the Q-point. What is the operating region of the transistor?

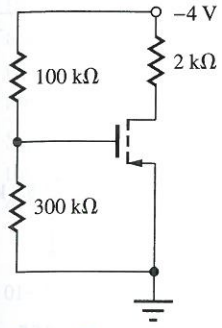

Figure P4.137

4.138. (a) Find the Q-point for the transistor in Fig. P4.138 if $R = 50$ kΩ. Assume that $\gamma = 0$ and $W/L = 20/1$. (b) What is the permissible range of values for R if the transistor is to remain in the saturation region?

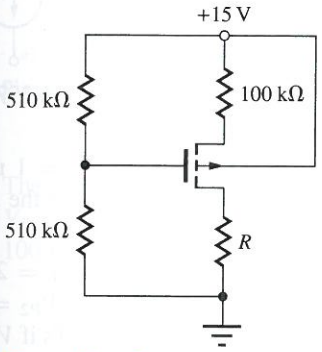

Figure P4.138

4.139. Simulate the circuit of Prob. 4.138(a) and find the Q-point. Compare the results to hand calculations.

*4.140. (a) Find the Q-point for the transistor in Fig. P4.138 if $R = 43$ kΩ. Assume that $\gamma = 0.5\sqrt{\text{V}}$ and $W/L = 20/1$. (b) What is the permissible range of values for R if the transistor is to remain in the saturation region?

4.141. Simulate the circuit of Prob. 4.140(a) and find the Q-point. Compare the results to hand calculations.

4.142. (a) Find the Q-point for the transistor in Fig. P4.142 if $V_{DD} = 14$ V, $R = 100$ kΩ, $W/L = 10/1$, and $\gamma = 0$. (b) Repeat for $\gamma = 1\sqrt{\text{V}}$.

4.143. Find the Q-point current for the transistor in Fig. P4.138 if all resistors are reduced by a factor of 2. Assume saturation region operation. What value of R is needed to set $V_{DS} = -5$ V. Assume that $\gamma = 0$ and $W/L = 40/1$.

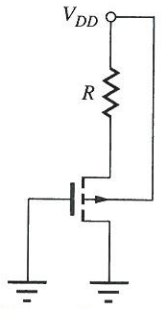

Figure P4.142

4.144. Repeat Prob. 4.143 if $\gamma = 0.5\sqrt{\text{V}}$ and $W/L = 40/1$.

4.145. (a) Find the Q-point current for the transistor in Fig. P4.138 if the upper 510-kΩ resistor is changed to 270 kΩ. Assume that the transistor is saturated, $\gamma = 0$, and $W/L = 20/1$. (b) What is the permissible range of values for R if the transistor is to remain in the saturation region?

4.146. Repeat Prob. 4.145 if $\gamma = 0.5\sqrt{\text{V}}$.

4.147. (a) Design a four-resistor bias network for a PMOS transistor to give a Q-point of (500 μA, −3 V) with $V_{DD} = -9$ V and $R_{EQ} \geq 1$ MΩ. Use the parameters from Table 4.6. (b) Repeat for an NMOS transistor with $V_{DS} = +3$ V and $V_{DD} = +9$ V.

4.148. (a) Design a four-resistor bias network for a PMOS transistor to give a Q-point of (1 mA, −5 V) with $V_{DD} = -15$ V and $R_{EQ} \geq 100$ kΩ. Use the parameters from Table 4.6. (b) Repeat for an NMOS transistor with $V_{DS} = +6$ V and $V_{DD} = +15$ V.

4.149. Find the Q-point for the transistor in Fig. P4.149 if $V_{TO} = +4$ V, $\gamma = 0$, and $W/L = 10/1$.

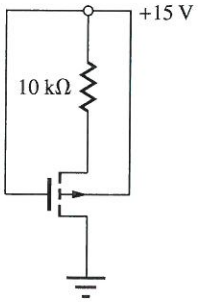

Figure P4.149

4.150. Find the Q-point for the transistor in Fig. P4.149 if $V_{TO} = +4$ V, $\gamma = 0.25\sqrt{\text{V}}$, and $W/L = 10/1$.

4.151. Find the Q-point for the transistor in Fig. P4.151 if $V_{TO} = -1$ V and $W/L = 10/1$.

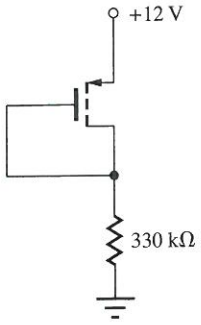

Figure P4.151

4.152. Find the Q-point for the transistor in Fig. P4.151 if $V_{TO} = -3$ V and $W/L = 30/1$.

4.153. What is the Q-point for each transistor in Fig. P4.153?

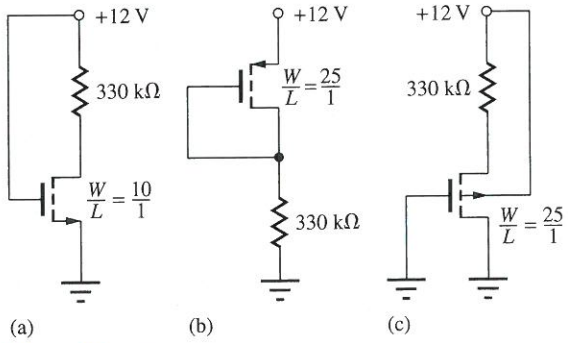

Figure P4.153

4.11 The Junction Field-Effect Transistor (JFET)

4.154. The JFET in Fig. P4.154 has $I_{DSS} = 500$ μA and $V_P = -3$ V. Find the Q-point for the JFET for (a) $R = 0$ and $V = 5$ V (b) $R = 0$ and $V = 0.25$ V, and (c) $R = 8.2$ kΩ and $V = 5$ V.

4.155. Find the Q-point for the JFET in Fig. P4.155 if $I_{DSS} = 5$ mA and $V_P = -5$ V.

4.156. Find the on-resistance of the JFET in Fig. P4.156 if $I_{DSS} = 1$ mA and $V_P = -5$ V. Repeat for $I_{DSS} = 100$ μA and $V_P = -2$ V.

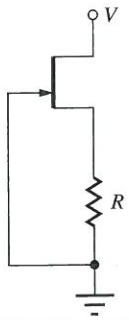

Figure 4.154

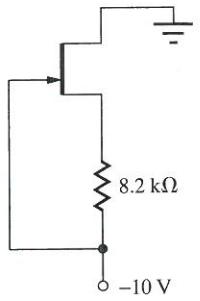

Figure 4.155

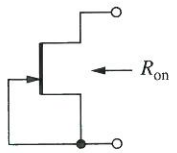

Figure 4.156

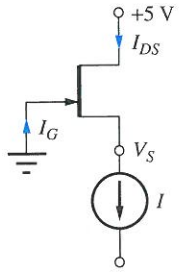

Figure 4.157

4.157. The JFET in Fig. P4.157 has $I_{DSS} = 1$ mA and $V_P = -4$ V. Find I_D, I_G, and V_S for the JFET if (a) $I = 0.5$ mA and (b) $I = 2$ mA.

*4.158. The JFETs in Fig. P4.158 have $I_{DSS1} = 200$ μA, $V_{P1} = -2$ V, $I_{DSS2} = 500$ μA, and $V_{P2} = -4$ V. (a) Find the Q-point for the two JFETs if $V = 9$ V. (b) What is the minimum value of V that will ensure that both J_1 and J_2 are in pinch-off?

*4.159. The JFETs in Fig. P4.159 have $I_{DSS} = 200$ μA and $V_P = +2$ V. (a) Find the Q-point for the two JFETs if $R = 10$ kΩ and $V = 15$ V. (b) What is the minimum value of V that will ensure that both J_1 and J_2 are in pinch-off if $R = 10$ kΩ?

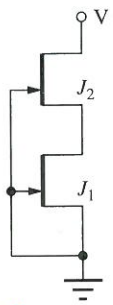

Figure 4.158

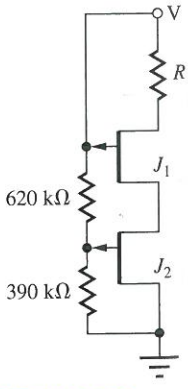

Figure 4.159

4.160. (a) The JFET in Fig. P4.160(a) has $I_{DSS} = 250\ \mu A$ and $V_P = -2$ V. Find the Q-point for the JFET. (b) The JFET in Fig. P4.160(b) has $I_{DSS} = 250\ \mu A$ and $V_P = +2$ V. Find the Q-point for the JFET.

4.161. Simulate the circuit in Prob. 4.160(a) and compare the results to hand calculations. (b) Repeat for Prob. 4.160(b).

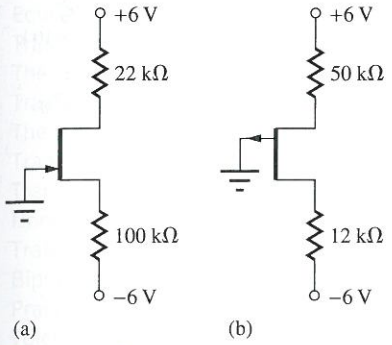

Figure 4.160

4.162. The JFET in Fig. P4.161 has $I_{DSS} = 250\ \mu A$ and $V_P = -2$ V. Find the Q-point for JFET for (a) $R = 100$ kΩ and (b) $R = 10$ kΩ.

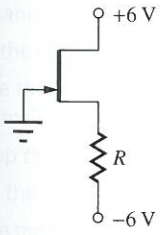

Figure 4.161

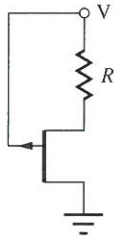

Figure 4.162

4.163. The JFET in Fig. P4.162 has $I_{DSS} = 500\ \mu A$ and $V_P = +3$ V. Find the Q-point for JFET for (a) $R = 0$ (b) $R = 10$ kΩ, and (c) $R = 100$ kΩ.

4.164. Simulate the circuit in Prob. 4.158(a) and compare the results to hand calculations.

4.165. Simulate the circuit in Prob. 4.159(a) and compare the results to hand calculations.

4.166. Use SPICE to plot the i-v characteristic for the circuit in Fig. P4.158 for $0 \le V \le 15$ V if the JFETs have $I_{DSS1} = 200\ \mu A$, $V_{P1} = -2$ V, $I_{DSS2} = 500\ \mu A$, and $V_{P2} = -4$ V.

4.167 The circuit in Fig. P4.167 is a voltage regulator utilizing an ideal op amp. (a) Find the output voltage of the circuit if the Zener diode voltage is 5 V. (b) What are the current in the Zener diode and the drain current in the NMOS transistor? (c) What is the op amp output voltage if the MOSFET has $V_{TN} = 1.25$ V and $K_n = 150\ \text{mA/V}^2$?

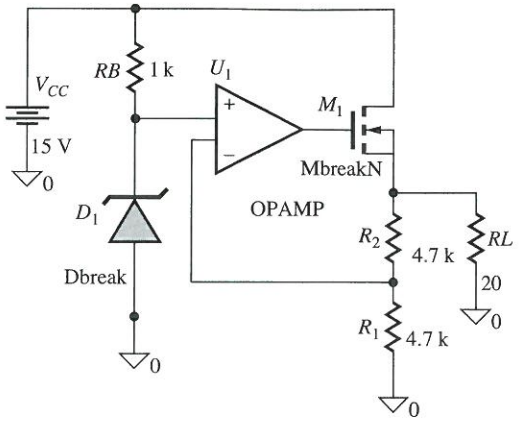

Figure 4.167

4.168 The circuit in Fig. P4.168 is a current regulator utilizing an ideal op amp. (a) Find the current in the Zener diode and the drain current in the NMOS transistor if the Zener voltage is 6.8 V. (b) What is the op amp output voltage if the MOSFET has $V_{TN} = 1.25$ V and $K_n = 75\ \text{mA/V}^2$?

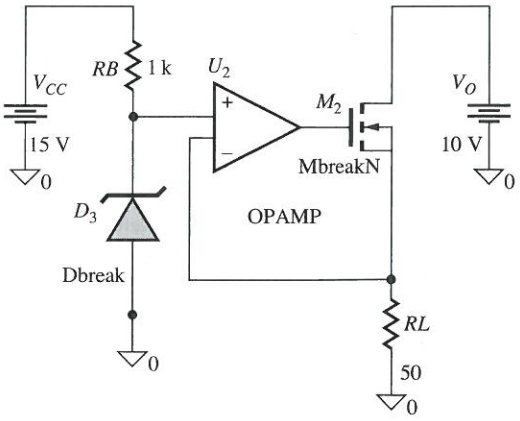

Figure 4.168

4.169 The circuit in Fig. P4.169 is a voltage regulator utilizing an ideal op amp. (a) Find the output voltage of the circuit if the Zener diode voltage is 5 V. (b) What are the current in the Zener diode and the drain current in the PMOS transistor? (c) What is the op amp output voltage if the MOSFET has $V_{TP} = -1.5$ V and $K_n = 50$ mA/V^2?

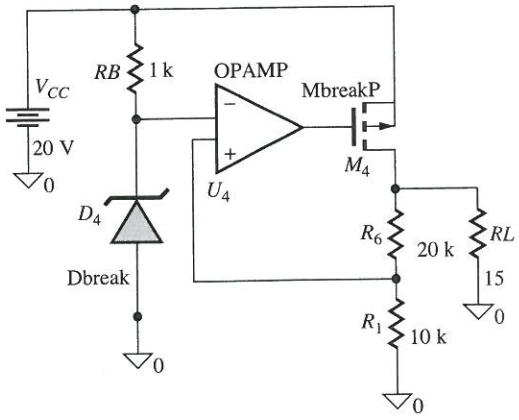

Figure 4.169