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2. J. R. Houser, "Noise margin criteria for digital logic circuits," *IEEE Trans. on Education,* vol. 36, no. 4, pp. 363–368, November 1993.
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5. J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE J. of Solid-State Circuits,* vol. 35, no. 10, pp. 1515–1516, October 2000.
6. R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," *IEEE J. of Solid-State Circuits,* vol. SC-7, no. 2, pp. 146–153, April 1972.
7. G. Boole, *An Investigation of the Laws of Thought, on Which Are Founded the Mathematical Theories of Logic and Probability,* 1849. Reprinted by Dover Publications, Inc., New York: 1954.

ADDITIONAL READING

Nelson, V. P., et al. *Analysis and Design of Logic Circuits*. Prentice-Hall, Englewood Cliffs, N.J.: 1995.

PROBLEMS

Use $K_n' = 100\ \mu A/V^2$, $K_p' = 40\ \mu A/V^2$, $V_{TN} = 0.6$ V, and $V_{TP} = -0.6$ V unless otherwise indicated.

General Introduction

6.1. Integrated circuit chips packaged in plastic can typically dissipate only 1 W per chip. Suppose we have an IC design that must fit on one chip and requires 100,000 logic gates. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 2.5 V is used, how much current can be used by each gate? Assume a 50 percent duty cycle.

6.2. A high-performance microprocessor design requires 100 million logic gates and is placed in a package that can dissipate 100 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 2.5 V is used, how much current can be used by each gate? Assume a 25 percent duty cycle. (c) What is the total current required by the IC chip?

Ideal Gates, Logic Level Definitions, and Noise Margins

6.3. (a) The ideal inverter in Fig. 6.2(b) has $R = 100$ kΩ and $V_+ = 2.5$ V. What are V_H and V_L? What is the power dissipation of the gate for $v_O = V_H$ and $v_O = V_L$? (b) Repeat for $V_+ = 3.3$ V.

6.4. Plot a graph of the voltage transfer characteristic for an ideal inverter with $V_+ = 2.5$ V, $V_- = 0$ V, and $V_{REF} = 0.8$ V. Assume $V_H = V_+$ and $V_L = V_-$.

6.5. (a) Plot a graph of the overall voltage transfer function for two cascaded ideal inverters if each individual inverter has a voltage transfer characteristic as defined in Prob. 6.4. (b) What is the overall logic expression $Z = f(A)$ for the two cascaded inverters?

6.6. Plot a graph of the voltage gain A_v of the ideal inverter in Fig. 6.1 as a function of input voltage v_I. $(A_v = dv_O/dv_I)$

6.7. The voltage transfer characteristic for an inverter is given in Fig. P6.7. What are V_H, V_L, V_{IH}, V_{IL}? Plot the voltage gain A_v of the inverter $(A_v = dv_O/dv_I)$ as a function of v_I.

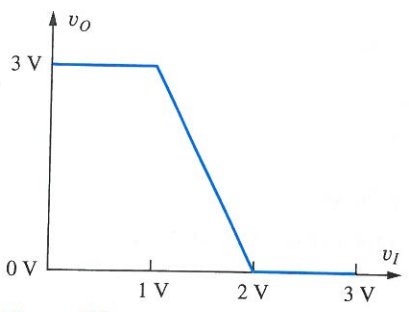


Figure P6.7

6.8. Plot a graph of the overall voltage transfer characteristic for two cascaded inverters if each individual inverter has the voltage transfer function defined in Fig. P6.7.

6.9. Suppose $V_H = 5$ V, $V_L = 0$ V, and $V_{REF} = 2.0$ V for the ideal logic gate in Fig. 6.1. What are the values of V_{IH}, V_{OL}, V_{IL}, V_{OH}, NM_H, and NM_L?

6.10. Suppose $V_H = 3.3$ V and $V_L = 0$ V for the ideal logic gate in Fig. 6.1. Considering noise margins, what would be the best choice of V_{REF}, and why did you make this choice?

6.11. The static voltage transfer characteristic for a practical CMOS inverter is given in Fig. P6.11. Estimate the values of V_H, V_L, V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_H, and NM_L.

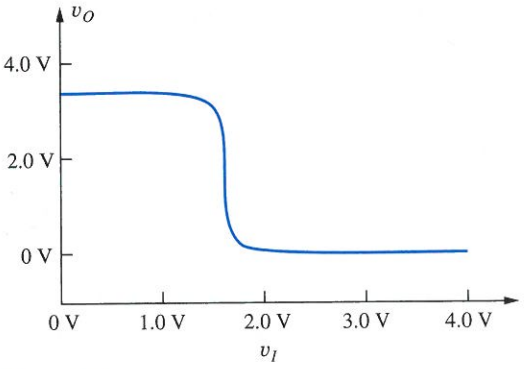


Figure P6.11

6.12. The graph in Fig. P6.12 gives the results of a SPICE simulation of an inverter. What are V_H and V_L for this gate?

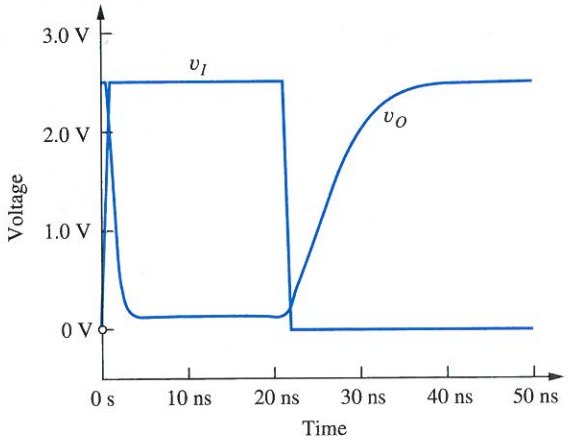


Figure P6.12

6.13. The graph in Fig. P6.13 gives the results of a SPICE simulation of an inverter. What are V_H and V_L for this gate?

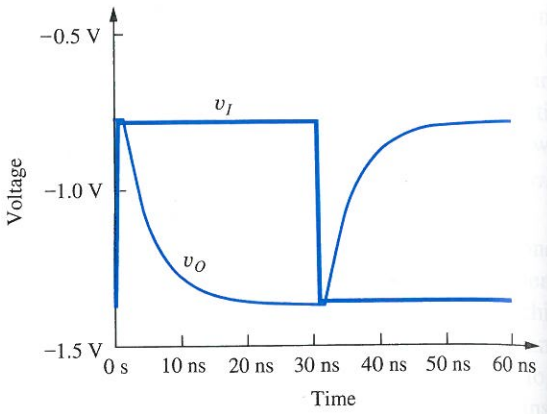


Figure P6.13

6.14. An ECL gate exhibits the following characteristics: $V_{OH} = -0.8$ V, $V_{OL} = -2.0$ V, and $NM_H = NM_L = 0.5$ V. What are the values of V_{IH} and V_{IL}?

Dynamic Response of Logic Gates

6.15. A logic family has a power-delay product of 100 fJ. If a logic gate consumes a power of 100 μW, estimate the propagation delay of the logic gate.

6.16. Plot the power-delay product versus power for the logic gate with the power-delay characteristic depicted in Fig. 6.6.

6.17. A 1-GHz processor has 10^9 logic gates with an average propagation delay of 150 ps. If the package can dissipate 50 W, what is the average power per gate assuming a 33 percent duty cycle? What is the power-delay product?

6.18. Integrated circuit chips packaged in plastic can typically dissipate only 1 W per chip. Suppose we have an IC design that must fit on one chip and requires 500,000 logic gates. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 2.5 V is used, how much current can be used by each gate? Assume a 50 percent duty cycle. (c) If the average gate delay for these circuits must be 2 ns, what is the power-delay product required for the circuits in this design?

6.19. A high-performance microprocessor design requires 200 million logic gates and is placed in a package that can dissipate 100 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 1.8 V is used, how much current can be used by each gate? Assume a 20 percent duty cycle. (c) If the average gate delay for these circuits must be 1 ns, what is

the power-delay product required for the circuits in this design?

*6.20. (a) Derive an expression for the rise time of the circuit in Fig. P6.20(a) in terms of the circuit time constant. Assume that $v(t)$ is a 1-V step function, changing state at $t = 0$. (b) Derive a similar expression for the fall time of the capacitor voltage in Fig. P6.20(b) if the capacitor has an initial voltage of 1 V at $t = 0$.

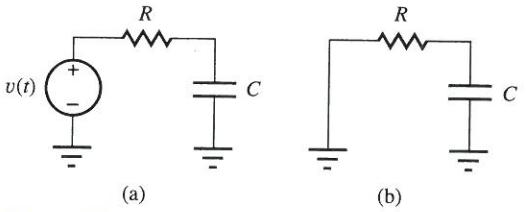


Figure P6.20

6.21. The graph in Fig. P6.12 gives the results of a SPICE simulation of an inverter. (a) What are V_H and V_L for this gate? (b) What are the rise and fall times for v_I and v_O? (c) What are the values of τ_{PHL} and τ_{PLH}? (d) What is the average propagation delay for this gate?

6.22. The graph in Fig. P6.13 gives the results of a SPICE simulation of an inverter. (a) What are V_H and V_L for this gate? (b) What are the rise and fall times for v_I and v_O? (c) What are the values of τ_{PHL} and τ_{PLH}? (d) What is the average propagation delay for this gate?

6.4 Review of Boolean Algebra

6.23. Use the results in Table 6.2 to prove that $(A + B) \cdot (A + C) = A + BC$.

6.24. Use the results in Table 6.2 to simplify the logic expression $Z = \bar{A}\bar{B}C + ABC + \bar{A}BC + A\bar{B}C$.

6.25. Make a truth table for the expression in Prob. 6.24.

6.26. Use the results in Table 6.2 to simplify the logic expression $Z = AB\bar{C} + ABC + \bar{A}BC$.

6.27. Make a truth table for the expression in Prob. 6.26.

6.28. Make a truth table and write an expression for the two logic functions in Fig. P6.28.

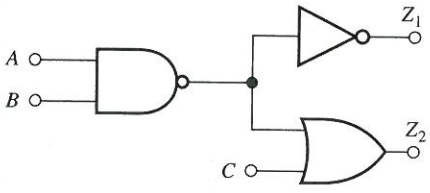


Figure P6.28

6.29. Make a truth table and write an expression for the logic function in Fig. P6.29.

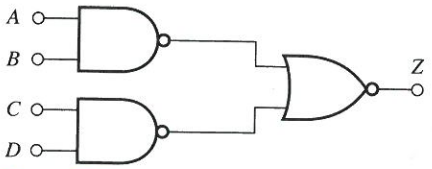


Figure P6.29

6.30. (a) What is the fan out of the NAND gate in Fig. P6.28? (b) Of each NAND gate in Fig. P6.29?

General Problems

6.31. A high-speed microprocessor must drive a 64-bit data bus in which each line has a capacitive load C of 40 pF, and the logic swing is 3.3 V. The bus drivers must discharge the load capacitance from 3.3 V to 0 V in 0.8 ns, as depicted in Fig. P6.31. Draw the waveform for the current in the output of the bus driver as a function of time for the indicated waveform. What is the peak current in the microprocessor chip if all 64 drivers are switching simultaneously?

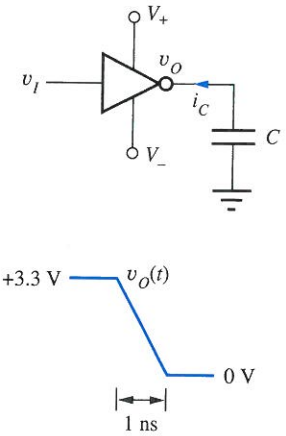


Figure P6.31 Bus driver and switching waveform.

6.32. Repeat Prob. 6.31 for a processor with a 1-GHz clock. Assume that the fall time must be 0.1 ns instead of 1 ns, as depicted in Fig. P6.31.

*6.33. A particular interconnection between two logic gates in an IC chip runs one-half the distance across a 7.5-mm-wide die. The interconnection line is insulated from the substrate by silicon dioxide. If the line is 1.5 μm wide and the oxide ($\varepsilon_{ox} = 3.9\varepsilon_o$ and $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm) beneath the line is

1 μm thick, what is the total capacitance of this line assuming that the capacitance is three times that predicted by the parallel plate capacitance formula? Assume that the silicon beneath the oxide represents a conducting ground plane.

**6.34. Ideal constant-electric-field scaling of a MOS technology reduces all the dimensions and voltages by the same factor α. Assume that the circuit delay ΔT can be estimated from

$$\Delta T = C\frac{\Delta V}{I}$$

in which the capacitance C is proportional to the total gate capacitance of the MOS transistor, $C = C''_{ox}WL$, ΔV is the logic swing, and I is the MOSFET drain current in saturation. Show that constant-field scaling results in a reduction in delay by a factor of α and a reduction in power by a factor of α^2 so that the PDP is reduced by a factor of α^3. Show that the power density actually remains constant under constant-field scaling.

**6.35 For many years, MOS devices were scaled to smaller and smaller dimensions without changing the power supply voltage. Suppose that the width W, length L, and oxide thickness T_{ox} of a MOS transistor are all reduced by a factor of 2. Assume that V_{TN}, v_{GS}, and v_{DS} remain the same. (a) Calculate the ratio of the drain current of the scaled device to that of the original device. (b) By what factor has the power dissipation changed? (c) By what factor has the value of the total gate capacitance changed? (d) By what factor has the circuit delay ΔT changed? (Use the delay formula in Prob. 6.34)

6.5 NMOS Logic Design

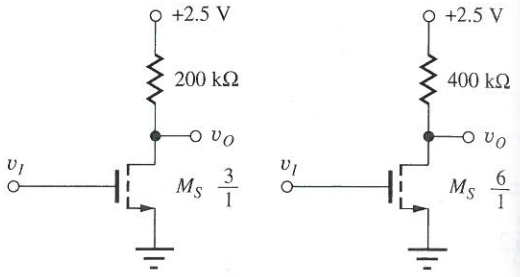
6.36. Integrated circuit chips packaged in plastic DIPs (dual-in-line packages) can typically dissipate 1 W per chip. Suppose that we have an IC design that must fit on one chip and requires two million logic gates. Assume that one-third the logic gates on the chip are conducting current at any given time. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 1.8 V is used, how much current can be used by each gate?

6.37. A high-performance microprocessor design requires 20 million logic gates and will be placed in a package that can dissipate 20 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 1.8 V is used, how much current can be used by each gate? Assume that one-third of the logic gates on the chip are in the conducting state at any given time.

Resistor Load Inverter

6.38. Design a resistive load inverter to operate from a 2.0-V power supply with a power dissipation of 50 μW.

6.39. (a) Find V_H, V_L, and the power dissipation (for $v_O = V_L$) for the logic inverter with resistor load in Fig. P6.39(a). (b) Repeat for Fig. P6.39(b).



(a) (b)

Figure P6.39

6.40. (a) What should be the value of W/L for the transistor in Fig. 6.39(b) if it is to have the same value of V_L as the inverter in Fig. 6.39(a)? (a) What should be the value of W/L for the transistor in Fig. 6.39(a) if it is to have the same value of V_L as the inverter in Fig. 6.39(b)?

6.41. (a) The load resistor in Fig. 6.39(a) is changed to 100 kΩ. What should be the new value of W/L if V_L is to remain unchanged? (b) What is the new value of V_H? (c) The load resistor in Fig. 6.39(b) is changed to 200 kΩ. What should be the new value of W/L if V_L is to remain unchanged?

6.42. A manufacturing problem caused $V_{TN} = 0.8$ V instead of 0.6 V for the inverter in Fig. P6.39(a). (a) What are the values of V_H, V_L, and power dissipation? (b) Repeat for $V_{TN} = 0.4$ V.

6.43. (a) What are the noise margins for the circuit in Fig. P6.39(a)? (b) Fig. P6.39(b)?

6.44. (a) Find V_H, V_L, and the power dissipation (for $v_O = V_L$) for the logic inverter with resistor load in Fig. P6.39(b). (b) A manufacturing problem caused $V_{TN} = 0.5$ V instead of 0.6 V. What are the new values of V_H, V_L, and power dissipation? (c) Repeat for $V_{TN} = 0.7$ V.

6.45. (a) What is the minimum value of K_nR required for both noise margins to be positive in the inverter in Ex. 6.4? (b) What is V_L for this value of K_nR? (c) What value of W/L corresponds to the value of

$K_n R$ in part (a)? (d) What is the value of R_{on} for the transistor?

6.46. (a) What are the noise margins for the circuit in Fig. P6.39(b)? (b) What value of W/L will result in $N_{ML} = 0$ for the resistive load inverter in Fig. P6.39(b)?

6.47. Plot the noise margins of the inverter in Ex. 6.4 as a function of W/L of the switching transistor.

6.48. Find the nominal and worst-case values for the noise margins of the inverter in Ex. 6.4 if the threshold voltage has a tolerance of 10 percent, the power supply has a 5 percent tolerance, and K_n and R both have 30 percent tolerances.

6.49. (a) Perform a 1000 case Monte Carlo analysis for the noise margins of the inverter in Ex. 6.4 if the threshold voltage has a tolerance of 10 percent, the power supply has a 5 percent tolerance and K_n and R both have 30 percent tolerances. What are the nominal, minimum and maximum values of NM_L and NM_H? (b) Compare the results to those of Prob. 6.48.

6.50. The resistive load inverter in Fig. 6.12 is to be redesigned for $V_L = 0.5$ V. (a) What are the new values of R and $(W/L)_S$ assuming that the power dissipation remains the same? (b) What are the values of NM_L and NM_H?

6.51. (a) Redesign the resistive load inverter of Fig. 6.12 for operation at a power level of 0.30 mW with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.7$ V. Keep the other design parameters the same. What is the new size of M_S and the value of R? (b) What are the values for NM_H and NM_L?

6.52. (a) Design an inverter with a resistive load for $V_{DD} = 2.0$ V and $V_L = 0.15$ V. Assume $I_{DD} = 10$ μA, $K_n' = 75$ μA/V^2, and $V_{TN} = 0.6$ V. (b) Confirm the validity of your design with SPICE.

6.53. Design an inverter with a resistive load for $V_{DD} = 3$ V and $V_L = 0.30$ V. Assume $I_{DD} = 33$ μA, $K_n' = 60$ μA/V^2, and $V_{TN} = 0.75$ V. (b) Confirm the validity of your design with SPICE.

6.6 Transistor Alternatives to Resistor Load

6.54. (a) Calculate the on-resistance of an NMOS transistor with $W/L = 10/1$ for $V_{GS} = 5$ V, $V_{SB} = 0$, $V_{TO} = 1$ V, and $V_{DS} = 0$ V. (b) Calculate the on-resistance of a PMOS transistor with $W/L = 10/1$ for $V_{SG} = 5$ V, $V_{SB} = 0$, $V_{TO} = -1$ V, and $V_{SD} = 0$ V. (c) What do we mean when we say that a transistor is "on" even though I_D and $V_{DS} = 0$? (d) What must be the W/L ratios of the NMOS and PMOS transistors if they are to have the same on-resistance as parts (a) and (b) with $|V_{GS}| = 3.0$ V?

Saturated Load Inverter

6.55. Find V_H for an NMOS logic gate with a saturated load if $V_{TO} = 0.5$ V, $\gamma = 0.85\ \sqrt{\text{V}}$, $2\phi_F = 0.6$ V, and $V_{DD} = 2.5$ V.

6.56. Find V_H for an NMOS logic gate with a saturated load if $V_{TO} = 0.75$ V, $\gamma = 0.75\ \sqrt{\text{V}}$, $2\phi_F = 0.7$ V, and $V_{DD} = 3.0$ V.

6.57. Find V_H for an NMOS logic gate with a saturated load if $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, $2\phi_F = 0.6$ V, and $V_{DD} = 3.3$ V.

6.58. Suppose there is a 30 percent tolerance on the value of K_n' in the inverter in Fig. 6.21. What are the worst-case values of V_H, V_L, and the power in the circuit? Assume the two transistors in the circuit are matched (i.e., they have the same value of K_n').

6.59. Find V_H, V_L, and the power dissipation (for $v_O = V_L$) for the logic inverter with the saturated load in Fig. P6.59. Assume $\gamma = 0$.

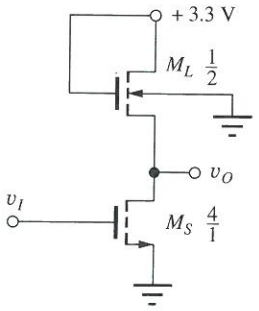


Figure P6.59

6.60. Repeat Prob. 6.59 if $\gamma = 0.6$.

6.61. Suppose there is a 30 percent tolerance on the value of K_n' in the inverter in Fig. P6.59. What are the worst-case values of V_H, V_L and the power in the circuit? Assume the two transistors in the circuit are matched (i.e., they have the same value of K_n').

6.62. A manufacturing problem caused $V_{TN} = 0.8$ V instead of 0.6 V in the inverter in Fig. P6.59. What are the new values of V_H, V_L, and power dissipation? (c) Repeat for $V_{TN} = 0.4$ V.

*6.63. What are the noise margins for the circuit in Fig. P6.59?

6.64. (a) Find V_H, V_L, and the power dissipation (for $v_o = V_L$) for the logic inverter with the saturated load in Fig. P6.59 if the transistor sizes are changed

to $(W/L)_S = 8/1$ and $(W/L)_L = 1/1$. (b) What are the noise margins for the circuit? (c) A manufacturing problem caused $V_{TN} = 0.7$ V instead of 0.6 V. What are the new values of V_H, V_L, and power dissipation?

6.65. Redesign the NMOS logic gate with saturated load of Fig. 6.21 to give $V_L = 0.3$ V and $P = 0.4$ mW for $v_O = V_L$.

6.66. (a) Redesign the saturated load inverter of Fig. 6.21 for operation at a power level of 0.25 mW with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.7$ V. Keep the other design parameters the same. What are the new sizes of M_L and M_S? (b) What are the new values for NM_H and NM_L?

6.67. (a) Design a saturated load inverter similar to that of Fig. 6.17(c) with $V_{DD} = 3.3$ V and $V_L = 0.2$ V. Assume $I_{DD} = 75\ \mu$A. (b) Recalculate the values of W/L including body effect, as in Fig. 6.21.

6.68. (a) Design a saturated load inverter similar to that of Fig. 6.17(c) with $V_{DD} = 2.0$ V and $V_L = 0.15$ V. Assume $I_{DD} = 25\ \mu$A and $V_{TN} = 0.6$ V. (b) Recalculate the values of W/L including body effect, as in Fig. 6.21 if $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V. (c) Confirm the validity of your designs with SPICE.

6.69. The logic input of the saturated load inverter of Fig. 6.21 is connected to 2.5 V. What is v_O for this input voltage? (This problem will probably require an iterative solution.)

6.70. The saturated load inverter of Fig. 6.29(b) was designed using $K_n' = 100\ \mu\text{A/V}^2$, but due to process variations during fabrication, the value actually turned out to be $K_n' = 125\ \mu\text{A/V}^2$. What will be the new values of V_H, V_L, and the power dissipation in the gate for this new value of K_n'?

6.71. The saturated load inverter of Fig. 6.29(b) was designed using $K_n' = 100\ \mu\text{A/V}^2$, but due to process variations during fabrication, the value actually turned out to be $K_n' = 75\ \mu\text{A/V}^2$. What will be the new values of V_H, V_L, and the power dissipation in the gate for this new value of K_n'?

6.72. The inverter designs in Fig. 6.29 assume $\lambda = 0$. (a) Does V_H depend upon the value of λ? (b) Use SPICE to find I_{DD} and V_L for the saturated load inverter in Fig. 6.29(b) if $\lambda = 0.02$, 0.05, and 0.1 V^{-1}.

**6.73. Plot the noise margins for the saturated load inverter similar to the design of Fig. 6.29(b) versus $K_R = K_S/K_L$ (see the graph in Fig. 6.28). Note that V_L will be changing.

6.74. Find the slope of the voltage transfer characteristic (i.e., the voltage gain) at the input voltage for which $v_O = v_I$ in the inverter in Fig. 6.21.

6.75. Find the slope of the voltage transfer characteristic (i.e., the voltage gain) at the input voltage for which $v_O = v_I$ in the inverter in Fig. P6.59.

NMOS Inverter with a Linear Load Device

6.76. Calculate the W/L ratio for the linear load device using the circuit and device parameters that apply to Sec. 6.8, and show that the values presented in Fig. 6.22 are correct.

6.77. What is the minimum value of V_{GG} required for linear region operation of M_L in Fig. 6.29(c) if $V_{TO} = 0.8$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V.

6.78. The linear load inverter in Fig. 6.29(c) was designed using $K_n' = 100\ \mu\text{A/V}^2$. (a) What will be the new values of V_H, V_L, and the power dissipation in this gate if $K_n' = 70\ \mu\text{A/V}^2$? (b) Repeat for $K_n' = 130\ \mu\text{A/V}^2$.

6.79. Find V_H, V_L, and the power dissipation (for $v_O = V_{OL}$) for the linear load inverter in Fig. P6.79.

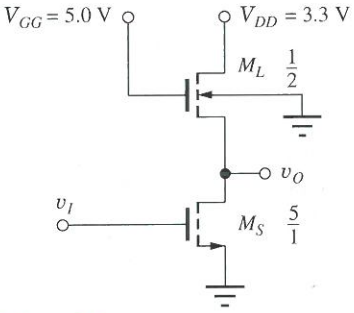


Figure P6.79

6.80. What is the minimum value of V_{GG} in the circuit in Fig. P6.79 if $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V.

6.81. The linear load inverter in Fig. P6.79 was designed using $K_n' = 100\ \mu\text{A/V}^2$. (a) What will be the new values of V_H, V_L and the power dissipation in this gate if $K_n' = 130\ \mu\text{A/V}^2$? (b) Repeat for $K_n' = 70\ \mu\text{A/V}^2$.

6.82. (a) Design a linear load inverter similar to that of Fig. P6.79 with $V_{DD} = 3.3$ V, $V_L = 0.20$ V, and $P = 300\ \mu$W. Assume $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, $2\phi_F = 0.6$ V. (b) Confirm the validity of your design using SPICE.

6.83. Repeat Probs. 6.79 and 6.80 if V_{DD} and V_{GG} are changed to 2.5 V and 3.5 V respectively.

NMOS Inverter with a Depletion-Mode Load

6.84. We know that body effect deteriorates the behavior of NMOS logic gates with depletion-mode loads. Assume that the depletion-mode load device has $V_{TO} = -1$ V and is operating in an inverter circuit with $V_{DD} = 2.5$ V. What is the largest value of the body-effect parameter γ that still will allow $V_{OH} = V_{DD}$? Assume $2\phi_F = 0.6$ V.

6.85. (a) Redesign the inverter with depletion-mode load of Fig. 6.29(d) for operation with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.6$ V for the switching transistor and $V_{TO} = -1$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V for the depletion-mode load. Design for $V_L = 0.20$ V and $P = 0.25$ mW.

6.86. (a) The depletion load inverter of Fig. 6.29(d) was designed using $K_n' = 100\ \mu\text{A/V}^2$, but due to process variations during fabrication, the value actually turned out to be $K_n' = 80\ \mu\text{A/V}^2$. What will be the new values of V_H, V_L, and the power dissipation in the gate for this new value of K_n'? (b) Repeat for $K_n' = 120\ \mu\text{A/V}^2$.

6.87. (a) Design a depletion-load inverter to operate with $V_{DD} = 3.3$ V, $V_L = 0.20$ V, and $P = 250\ \mu$W. Assume $V_{TO} = -2$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V for the load transistor and $V_{TO} = 0.6$ V for M_S. (b) Confirm the validity of your design using SPICE.

6.88. The inverter designs in Fig. 6.29 assume $\lambda = 0$. (a) Does V_H depend upon the value of λ? (b) Use SPICE to find I_{DD} and V_L for the depletion-load inverter in Fig. 6.29(d) if $\lambda = 0.02$, 0.05, and $0.1\ \text{V}^{-1}$.

6.89. Find the slope of the voltage transfer characteristic (i.e., the voltage gain) at the input voltage for which $v_O = v_I$ in the inverter in Fig. 6.29(d).

Pseudo NMOS Inverter

6.90. (a) The inverter in Fig. 6.29(e) is to be redesigned to have $V_L = 0.25$ V. What is the new value of $(W/L)_S$? (b) What are the noise margins for the new design?

6.91. (a) Due to process variations, the value of K_n' for the NMOS transistor in Fig. 6.29(e) was found to be $K_n' = 120\ \mu\text{A/V}^2$ instead of $100\ \mu\text{A/V}^2$. What are the new values of V_L and I_{DD}? (b) What are the new values of the noise margins? (c) Repeat parts (a) and (b) for $K_n' = 80\ \mu\text{A/V}^2$.

6.92. (a) Due to process variations, the NMOS threshold voltage for the inverter in Fig. 6.29(e) was found to be $V_{TN} = 0.5$ V instead of 0.6 V. What are the new values of V_L and I_{DD}? (b) What are the new values of the noise margins? (c) Repeat parts (a) and (b) for $V_{TN} = 0.7$ V.

6.93. (a) Due to process variations, the value of K_p' for the PMOS transistor in Fig. 6.29(e) was found to be $K_p' = 50\ \mu\text{A/V}^2$ instead of $40\ \mu\text{A/V}^2$. What are the new values of V_L and I_{DD}? (b) What are the new values of the noise margins? (c) Repeat parts (a) and (b) for $K_p' = 30\ \mu\text{A/V}^2$.

6.94. (a) Due to process variations, the PMOS threshold voltage for the inverter in Fig. 6.29(e) was found to be $V_{TP} = -0.5$ V instead of -0.6 V. What are the new values of V_L and I_{DD}? (b) What are the new values of the noise margins? (c) Repeat parts (a) and (b) for $V_{TP} = -0.7$ V.

6.95. (a) Design a pseudo NMOS inverter to operate from $V_{DD} = 1.8$ V with $V_L = 0.2$ V and a power of $100\ \mu$W. Assume $V_{TN} = 0.5$ V and $V_{TP} = -0.5$ V. (b) Find the noise margins for your design.

6.96. (a) Design a pseudo NMOS inverter to operate from $V_{DD} = 3.0$ V with $V_L = 0.3$ V and a power of $200\ \mu$W. (b) Find the noise margins for your design.

6.8 NMOS NAND and NOR Gates

6.97. (a) What is the value of V_L in the two-input NOR gate in Fig. 6.30(a) when both $A = 1$ and $B = 1$? (b) What is the current in V_{DD} for this input condition?

6.98. The design value for V_L was 0.2 V in the NAND gate in Fig. 6.32(a). What is the actual value of V_L?

6.99. Calculate the W/L ratios of the switching devices in the NAND gate in Fig. 6.32(b) and verify that they are correct.

**6.100. The two-input NAND gate in Fig. 6.32 was designed with equal values of R_{on} (approximately equal voltage drops) in the two series-connected switching transistors, but an infinite number of other choices are possible. Show that the equal R_{on} design requires the minimum total gate area for the switching transistors.

6.101. Draw the schematic for a four-input NAND gate with a depletion-mode load device. What are the W/L ratios of all the transistors, based on the reference inverter in Fig. 6.32?

6.102. Draw the schematic for a four-input NOR gate with a saturated load device. What are the W/L ratios of all the transistors, based on the reference inverter in Fig. 6.29?

6.103. (a) Draw the schematic for a three-input pseudo NMOS NOR gate. Choose the device sizes based upon the reference inverter in Fig. 6.29. (b) What is V_L if all the logic inputs are equal to 1?

6.104. (a) Draw the schematic for a three-input pseudo NMOS NAND gate. Choose the device sizes based upon the reference inverter in Fig. 6.29. Ignore body effect in your design. (b) What is V_L if all the logic inputs are equal to 1? Do not ignore body effect. (c) Redesign the sizes of the three switching transistors to account for body effect.

6.105. Draw the layout of a two-input NOR gate similar to that in Fig. 6.33(a) but use a saturated load device. Be sure to scale the transistor sizes properly based on Fig. 6.29(b).

6.106. (a) Draw the layout of a three-input NOR gate similar to that in Fig. 6.33(a). Be sure to scale the transistor sizes properly. (b) Draw the layout of a three-input NAND gate similar to that in Fig. 6.33(b). Be sure to scale the transistor sizes properly.

6.9 Complex NMOS Logic

6.107. (a) What is the logic function that is implemented by the gate in Fig. P6.107? (b) What are the W/L ratios for the transistors, based on the reference inverter design of Fig. 6.29(d)?

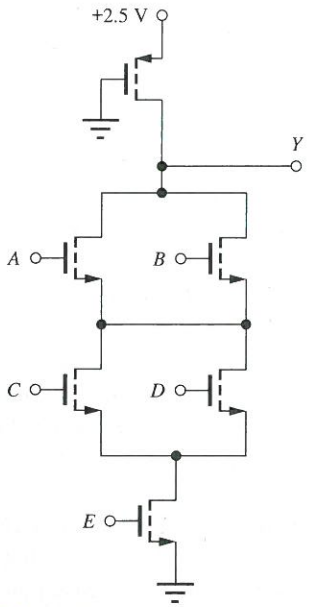


Figure P6.107

6.108. (a) Redraw the circuit in Fig. P6.107 using a saturated load transistor. (b) What is the logic function of the new circuit? (c) What are the W/L ratios of the transistors based upon the reference inverter design in Fig. 6.29(b)?

6.109. (a) What is the logic function that is implemented by the gate in Fig. P6.109? (b) What are the W/L ratios for the transistors, based on the reference inverter design of Fig. 6.29(d)?

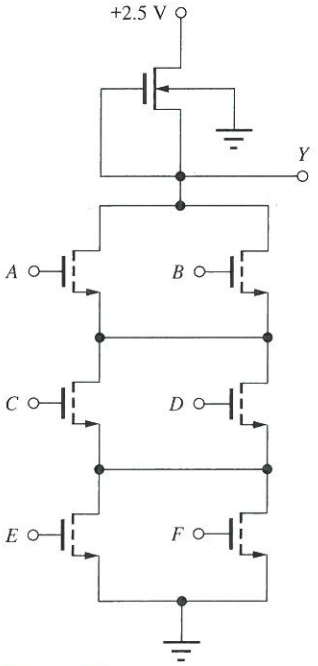


Figure P6.109

6.110. (a) Redraw the circuit in Fig. P6.109 using a saturated load transistor. (b) What is the logic function of the new circuit? (c) What are the W/L ratios of the transistors based upon the reference inverter design in Fig. 6.29(b)?

6.111. (a) What is the logic function that is implemented by the gate in Fig. P6.111? (b) What are the W/L ratios for the transistors if the gate is to dissipate three times as much power as the reference inverter design of Fig. 6.29(d)?

6.112. (a) Redraw the circuit in Fig. P6.111 using a saturated load transistor. (b) What is the logic function of the new circuit? (c) What are the W/L ratios of the transistors based on the reference inverter design in Fig. 6.29(b)?

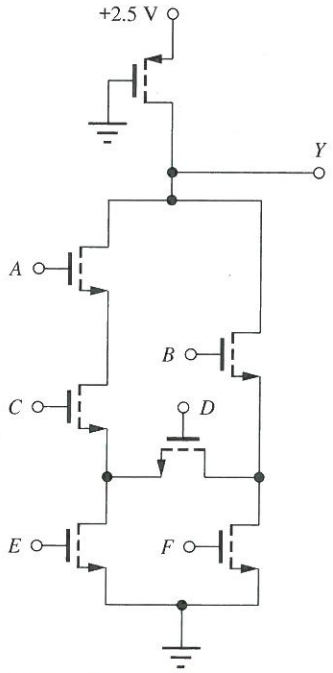


Figure P6.111

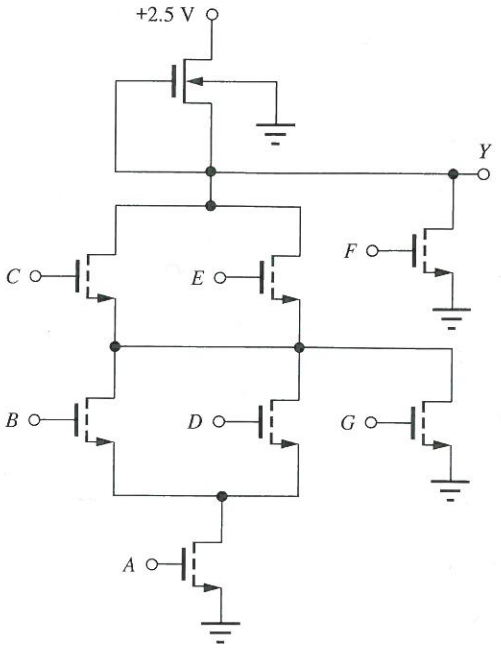


Figure P6.117

6.113. Design a depletion-load gate that implements the logic function $Y = \overline{A[B + C(D + E)]}$, based on the reference inverter design of Fig. 6.29(d).

6.114. Design a saturated-load gate that implements the logic function $Y = \overline{A(BC + DE)}$, based on the reference inverter design of Fig. 6.29(b).

6.115. Design a pseudo NMOS gate that implements the logic function $Y = \overline{A(BC + DE)}$ and consumes one-half the power of the reference inverter design of Fig. 6.29(e).

6.116. Design a pseudo NMOS gate that implements the logic function $Y = \overline{A(B + CD) + E}$, based on the reference inverter design of Fig. 6.29(e).

6.117. What is the logic function for the gate in Fig. P6.117? What are the W/L ratios of the transistors that form the gate if the gate is to consume twice as much power as the reference inverter in Fig. 6.29(d)?

6.118. (a) Design a depletion-load gate that implements the logic function $Y = \overline{A(B + CD) + E}$, based on the reference inverter design of Fig. 6.29(d). (b) Redesign the W/L ratios of this gate to account for body effect and differences in values of V_{DS} for the various transistors.

6.119. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.34 to account for the body effect and differences in the V_{DS} of the various transistors.

*6.120. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.35(a) to account for the body effect and differences in the V_{DS} of the various transistors.

*6.121. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.35(b) to account for the body effect and differences in the V_{DS} of the various transistors.

*6.122. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.36 to account for the body effect and differences in the V_{DS} of the various transistors.

**6.123. (a) What is the truth table for the logic function Y for the gate in Fig. P6.123? (b) Write an expression for the logical output of this gate. (c) What are the sizes of the transistors M_S and M_P in order for $V_L \leq 0.20$ V? (d) Qualitatively describe how the sizes of M_S and M_P will change if body effect is included in the models for the transistors. (e) What is the name for this logic function?

6.124. (a) Estimate the value of V_L in Fig. 6.36 if all five switching transistors are "on" by finding the equivalent value of R_{on} for the switching tree. (b) Compare your calculation to SPICE results.

6.10 Power Dissipation

6.125. Scale the sizes of the resistors and transistors in the five inverters in Fig. 6.29 to change the power dissipation level to 2 mW.

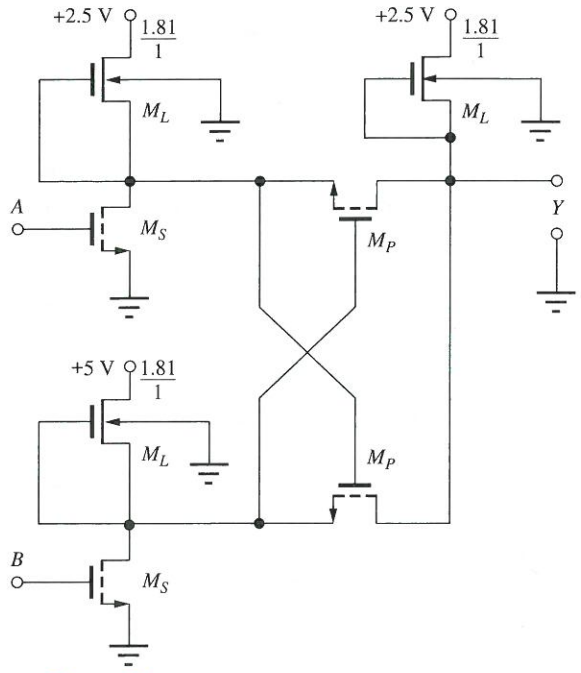


Figure P6.123

6.126. What are the W/L ratios of the transistors in the gate in Fig. P6.117 if the gate is to consume three times as much power as the reference inverter in Fig. 6.29(d)?

6.127. What are the W/L ratios for the transistors in Fig. P6.109 if the gate is to dissipate one-fifth as much power as the reference inverter design of Fig. 6.29(d)?

6.128. (a) Scale the transistor sizes in Fig. 6.35(a) to increase the gate power by a factor of four. (b) Scale the transistor sizes in Fig. 6.35(a) to decrease the gate power by a factor of four.

6.129. (a) Scale the transistor sizes in Fig. 6.35(b) to decrease the gate power by a factor of 8. (b) Scale the transistor sizes in Fig. 6.35(b) to increase the gate power by a factor of 3.5.

6.130. (a) Scale the transistor sizes in Fig. 6.36 to triple the gate power. (b) Scale the transistor sizes in Fig. 6.36 to decrease the gate power by a factor of four.

6.131. For the saturated load inverter, we found $V_H \neq V_{DD}$ and $V_L \neq 0$. Find a new general expression (similar to Eq. 6.49) for the dynamic power dissipation of a logic gate in terms of V_H, V_L and/or ΔV.

*6.132. For many years, MOS devices were scaled to smaller and smaller dimensions without changing the power supply voltage. Suppose that the width W, length L, and oxide thickness t_{ox} are all reduced by a factor of 2. Assume that V_{TN}, v_{GS}, and v_{DS} remain the same. Calculate the ratio of the drain current of the scaled device to that of the original device. How has the power dissipation changed?

6.133. A high-speed NMOS microprocessor has a 64-bit address bus and performs a memory access every 50 ns. Assume that all address bits change during every memory access, and that each bus line represents a load of 10 pF. (a) How much power is being dissipated by the circuits that are driving these signals if the power supply is 2.5 V? (b) 3.3 V?

6.11 Dynamic Behavior of MOS Logic Gates

6.134. A logic family has a power-delay product of 100 fJ. If a logic gate consumes a power of 100 μW, what is the expected propagation delay of the logic gate?

6.135. The graph in Fig. P6.135 gives the results of a SPICE simulation of an inverter. (a) What are the rise and fall times for v_I and v_O? (b) What are the values of τ_{PHL} and τ_{PLH}? (c) What is the average propagation delay for this gate?

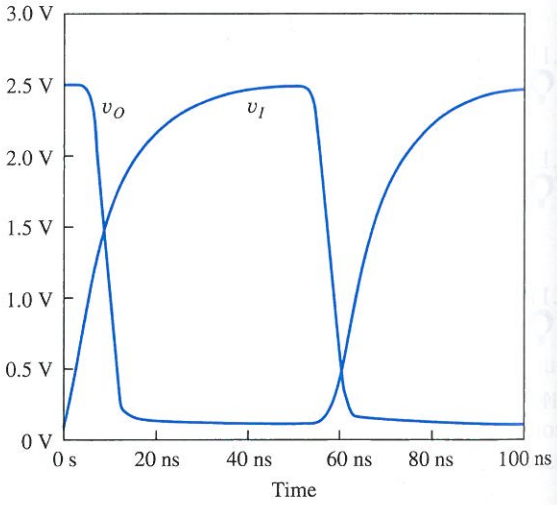


Figure P6.135

**6.136. Derive Eq. 6.63 for an N-stage ring oscillator by adding together the total number of τ_{PHL} and τ_{PLH} delays that occur in two round trips through the oscillator.

6.137. (a) Suppose that a ring oscillator contains 301 inverters and the average propagation delay of an inverter is 100 ps. What will be the period of the square wave generated by the oscillator? (b) What

is the frequency of oscillator? (c) Why should the number of inverters be odd? What could happen if an even number of inverters were used in the ring oscillator?

6.138. (a) The input capacitance for a gate can be written as $C_{in} = k_1 C_{GS} + k_2 C_{GD}$. Use SPICE to determine k_1 and k_2 for a resistively loaded NMOS logic gate. (b) Repeat for a psuedo NMOS circuit.

Resistor Load

6.139. What are the rise time, fall time, and average propagation delay of the NMOS gate in Fig. 6.12(b) if a load capacitance $C = 0.5$ pF is attached to the output of the gate?

6.140. What are the rise time, fall time, and average propagation delay of the NMOS gate in Fig. 6.12(b) if a load capacitance $C = 0.5$ pF is attached to the output of the gate and V_{DD} is increased to 3.3 V?

6.141. Design an NMOS inverter with resistor load to have an average propagation delay of 2.5 ns with a capacitive load of 1 pF by scaling the reference inverter based upon the results in Table 6.9. What is the average power dissipation of this gate with a 33 percent duty cycle?

6.142. Repeat Prob. 6.141 to achieve an average propagation delay of 2 ns with a 0.4 pF load. What is the average power dissipation of this gate with a 20 percent duty cycle?

6.143. Repeat the simulation of Ex. 6.10 with $\lambda = 0.04$/V. Compare the new values rise time, fall time, and propagation delays with those of the example.

Saturated Load

6.144. (a) What are the rise and fall times and average propagation delay of the NMOS gate in Fig. P6.144 if $C = 0.5$ pF and $V_{DD} = 2.5$ V? Use the estimates in Table 6.10. (b) What are the rise and fall times and average propagation delays of the NMOS gate in Fig. P6.144 if $C = 0.3$ pF and $V_{DD} = 3.3$ V? Use Table 6.10.

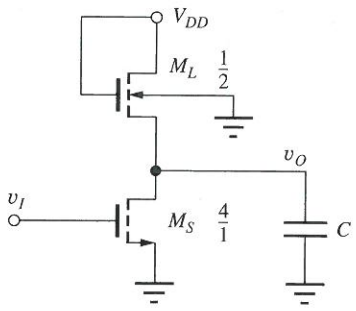


Figure P6.144

6.145. Design an NMOS saturated load inverter ($V_{DD} = 2.5$ V, $V_L = 0.25$ V) to have an average propagation delay of 2 ns with a capacitive load of 1 pF. What is the average static power dissipation of this gate? Make use of Table 6.9.

Linear Load

6.146. What are the rise and fall times and average propagation delay for the linear load inverter in Fig. 6.29(c) with a load capacitance of 0.7 pF? Use Table 6.10.

6.147. Use SPICE to determine the characteristics of the NMOS inverter with a linear load device for the design given in Fig. 6.29. (a) Simulate the voltage transfer function. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input and $C = 0.15$ pF.

Depletion-Mode Load

6.148. What are the sizes of the transistors in the NMOS depletion-mode load inverter if it must drive a 1-pF capacitance with an average propagation delay of 3 ns? Assume $V_{DD} = 3.0$ V and $V_L = 0.25$ V. What are the rise and fall times for the inverter? Use $V_{TNL} = -3$ V ($\gamma = 0$). Make use of Table 6.10.

6.149. Design an NMOS depletion load inverter ($V_{DD} = 3.3$ V, $V_L = 0.20$ V, $V_{TNS} = 0.75$ V, $V_{TNL} = -2$ V, $\gamma = 0$) to have an average propagation delay of 1 ns with a capacitive load of 0.2 pF. What is the average static power dissipation of this gate? Use the results in Table 6.9.

A Final Comparison of Load Devices

6.150. Currents in the various load devices are shown in Fig. 6.47. The resistor load has a value of 28.8 kΩ. The W/L ratios of the devices were chosen to set the current in each load device to 80 μA when $v_O = V_L = 0.20$ V. Calculate the values of the W/L ratios of the load devices that were used in the figure for the: (a) saturated load device including body effect, (b) saturated load device with no body effect, (c) linear load device including body effect, (d) linear load device with no body effect, (e) depletion-mode load device including body effect, (f) depletion-mode load with no body effect (g) pseudo NMOS load.

6.12 PMOS Problems

6.151. Design five PMOS logic gates similar to the ones in Fig. 6.29. Do not do a complete mathematical redesign, but design the PMOS circuits by scaling the W/L ratios in Fig. 6.29, assuming that $K_p' = 40\ \mu A/V^2$.

*6.152. What are the values of V_L and V_H for the inverter in Fig. P6.152?

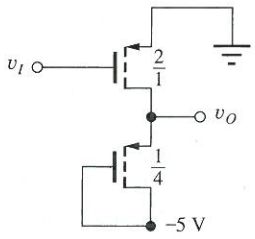


Figure P6.152

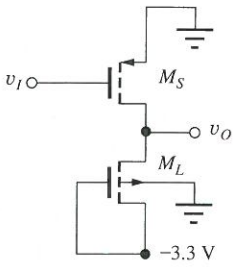


Figure P6.153

6.153. Design the transistors in the inverter of Fig. P6.153 so that $V_H = -0.33$ V and the power dissipation = 0.1 mW. Use the values in Table 6.5 on page 308.

6.154. What are the values of V_H and V_L for the inverter of Fig. P6.154? Use the values in Table 6.5 on page 308.

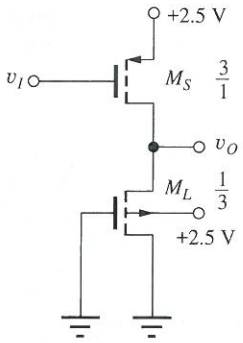


Figure P6.154

6.155. What is the logic function Y for the gate in Fig. P6.155?

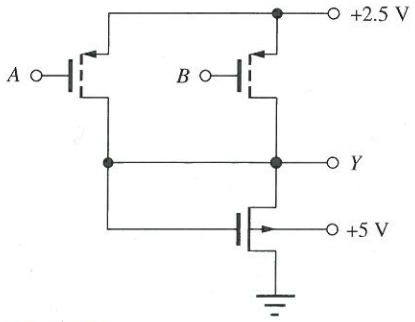


Figure P6.155

6.156. What is the logic function Y for the gate in Fig. P6.156?

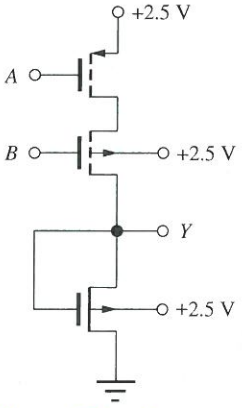


Figure P6.156

6.157. Simulate the voltage transfer characteristic for the PMOS gate in Fig. P6.152, and compare the results to those of Prob. 6.152.

6.158. Simulate the voltage transfer characteristic for the PMOS gate in Fig. P6.153, and compare the results to those of Prob. 6.153.

6.159. Simulate the delay of the PMOS gate in Fig. P6.152 with a load capacitance of 1 pF, and determine the rise time, fall time, and average propagation delay.

6.160. Simulate the delay of the PMOS gate in Fig. P6.153 with a load capacitance of 1 pF, and determine the rise time, fall time, and average propagation delay.