Precharge phase
Propagation delay
Rise time
Symmetrical CMOS inverter
Taper factor
Transmission gate

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PROBLEMS

Use $K_n' = 100\ \mu A/V^2$, $K_p' = 40\ \mu A/V^2$, $V_{TN} = 0.6$ V, and $V_{TP} = -0.6$ V unless otherwise indicated. *For simulation purposes, use the values in Appendix B.*

7.1 CMOS Inverter Technology

7.1. Calculate the values of K_n' and K_p' for NMOS and PMOS transistors with a gate oxide thickness of 100 Å. Assume that $\mu_n = 500\ cm^2/V \cdot s$, $\mu_p = 200\ cm^2/V \cdot s$, and the relative permittivity of the gate oxide is 3.9. ($\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm).

7.2. Draw a cross section similar to that in Fig. 7.1 for a CMOS process that uses a p-well instead of an n-well. Show the connections for a CMOS inverter, and draw an annotated version of the corresponding circuit schematic. (*Hint:* Start with an n-type substrate and interchange all the n- and p-type regions.)

*7.3. (a) The n-well in a CMOS process covers an area of 1 cm × 0.5 cm, and the junction saturation current density is 500 pA/cm^2. What is the total leakage current of the reverse-biased well? (b) Suppose the drain and source regions of the NMOS and PMOS transistors are 2 μm × 5 μm, and the saturation current density of the junctions is 100 pA/cm^2. If the chip has 20 million inverters, what is the total leakage current due to the reverse-biased junctions when $v_O = 2.5$ V? Assume $V_{DD} = 2.5$ V and $V_{SS} = 0$ V. (c) When $v_O = 0$ V?

*7.4. A particular interconnection between two logic gates in an IC chip runs one-half the distance across a 10-mm-wide die. If the line is 1 μm wide and the oxide ($\varepsilon_r = 3.9$, $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm) beneath the line is 1 μm thick, what is the total capacitance of this line, assuming that the capacitance is three times that predicted by the parallel plate capacitance formula? Assume that the silicon beneath the oxide represents a conducting ground plane.

7.5. The CMOS inverter in Fig. P7.5 has $V_{DD} = 2.5$ V and $V_{SS} = 0$ V. What are the values of V_H and V_L for this inverter? (b) Repeat for $V_{DD} = 1.8$ V.

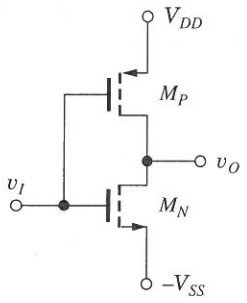


Figure P7.5

7.6. The CMOS inverter in Fig. P7.5 has $V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $(W/L)_N = 4/1$, and $(W/L)_P = 10/1$.

What are the values of V_H and V_L for this inverter? (b) Repeat for $(W/L)_N = 6/1$ and $(W/L)_P = 15/1$.

7.7. The CMOS inverter in Fig. P7.5 has $V_{DD} = 2.5$ V, $V_{SS} = 0$ V, $(W/L)_N = 4/1$, and $(W/L)_P = 10/1$. What are the values of V_H and V_L for this inverter? (b) Repeat for $(W/L)_N = 4/1$ and $(W/L)_P = 4/1$.

7.8. The CMOS inverter in Fig. P7.5 has $V_{DD} = 3.3$ V and $V_{SS} = 0$ V. If $V_{TN} = 0.75$ V and $V_{TP} = -0.75$ V, what are the regions of operation of the transistors for (a) $V_I = V_L$? (b) $V_I = V_H$? (c) $V_I = V_O = 1.65$ V?

7.9. The CMOS inverter in Fig. P7.5 has $V_{DD} = 2.5$ V and $V_{SS} = 0$ V. If $V_{TN} = 0.60$ V and $V_{TP} = -0.60$ V, what are the regions of operation of the transistors for (a) $V_I = V_L$? (b) $V_I = V_H$? (c) $V_I = V_O = 1.25$ V?

7.10. (a) The CMOS inverter in Fig. P7.5 with $(W/L)_N = 20/1$ and $(W/L)_P = 50/1$ is operating with $V_{DD} = 0$ V and $-V_{SS} = -5.2$ V. What are V_L and V_H? (b) If $(W/L)_N = 10/1$ and $(W/L)_P = 10/1$?

7.11. (a) Calculate the voltage at which $v_O = v_I$ for a CMOS inverter with $K_n = K_p$. (*Hint:* Always remember that $i_{DN} = i_{DP}$.) Use $V_{DD} = 2.5$ V, $V_{TN} = 0.6$ V, $V_{TP} = -0.6$ V. (b) What is the current I_{DD} from the power supply for $v_O = V_I$ if $(W/L)_N = 2/1$? (c) Repeat the calculation in (a) for a CMOS inverter with $K_n = 2.5K_p$. (d) What is the current I_{DD} from the power supply for $v_O = V_I$ if $(W/L)_N = 2/1$?

7.12. (a) Repeat Prob. 7.11 for $V_{DD} = 1.8$ V, $V_{TN} = 0.5$ V and $V_{TP} = -0.5$ V. (b) Repeat Prob. 7.11 for $V_{DD} = 2.5$ V, $V_{TN} = 0.75$ V and $V_{TP} = -0.65$ V. (c) Repeat Prob. 7.11 for $V_{DD} = 2.5$ V, $V_{TN} = 0.65$ V and $V_{TP} = -0.75$ V.

7.13. (a) Repeat Prob. 7.11 for $V_{DD} = 3.3$ V, $V_{TN} = 0.75$ V, and $V_{TP} = -0.75$ V. (b) Repeat Prob. 7.11 for $V_{DD} = 2.5$ V, $V_{TN} = 0.60$ V, and $V_{TP} = -0.50$ V.

7.2 Static Characteristics of the CMOS Inverter

7.14. Simulate the VTC for a CMOS inverter with $K_n = 2.5K_p$. Find the input voltage for which $v_O = v_I$ and compare to the value calculated by hand. Use $V_{DD} = 2.5$ V.

7.15. (a) The CMOS gate in Fig. P7.15 is called pseudo-NMOS. Find V_H and V_L for this gate. (b) Repeat for $V_{DD} = 2.5$ V. (c) Repeat for $V_{DD} = 1.8$ V.

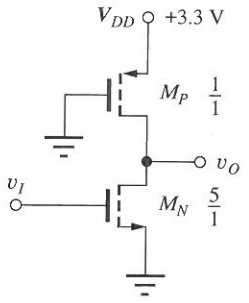


Figure P7.15

7.16 What is the switching threshold (where does $v_I = v_O$) for a minimum size inverter in which both W/L ratios are 2/1 if $V_{DD} = 2.5$ V and $V_{TN} = -V_{TP} = 0.6$ V?

7.17. What are the noise margins of a minimum size CMOS inverter in which both W/L ratios are 2/1 and $V_{DD} = 2.5$ V and $V_{TN} = -V_{TP} = 0.6$ V?

7.18. What is the switching threshold (where does $v_I = v_O$) for a minimum size inverter in which both W/L ratios are 2/1 if $V_{DD} = 1.8$ V and $V_{TN} = -V_{TP} = 0.5$ V?

7.19. What are the noise margins for a symmetrical CMOS inverter operating with $V_{DD} = 3.3$ V and $V_{TN} = -V_{TP} = 0.75$ V? (b) Repeat for a CMOS inverter having $(W/L)_N = (W/L)_P$ operating with $V_{DD} = 3.3$ V and $V_{TN} = -V_{TP} = 0.75$ V.

7.20. Use SPICE to plot the VTC for a CMOS inverter with $(W/L)_N = 2/1$, $(W/L)_P = 5/1$, $V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $V_{TN} = 0.75$ V, and $V_{TP} = -0.75$ V. Repeat if the threshold voltages are mismatched with values $V_{TN} = 0.85$ V and $V_{TP} = 0.65$ V. Repeat for $(W/L)_N = 2/1$ and $(W/L)_P = 4/1$ with the original threshold voltages. Plot the three curves on one graph.

7.21. (a) Plot a graph of the noise margins of the CMOS inverter (similar to Fig. 7.9) for $V_{DD} = 3.3$ V, $V_{TN} = 0.75$ V, and $V_{TP} = -0.75$ V. (b) Repeat for $V_{DD} = 2.0$ V, $V_{TN} = 0.50$ V, and $V_{TP} = -0.50$ V.

7.22. The outputs of two CMOS inverters are accidentally tied together, as shown in Fig. P7.22. What is the voltage at the common output node if the NMOS and PMOS transistors have W/L ratios of 20/1 and 40/1, respectively? What is the current in the circuit?

**7.23. A CMOS inverter is to be designed to drive a single TTL inverter (which will be studied in Chapter 9). When $v_O = V_L$, the CMOS inverter must

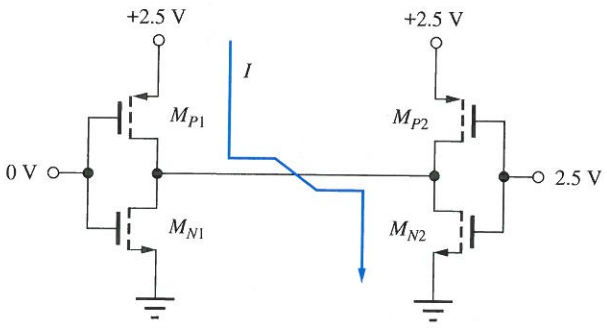


Figure P7.22

sink a current of 1.5 mA and maintain $V_L \leq 0.6$ V. When $v_O \geq V_H$, the CMOS inverter must source a current of 60 μA and maintain $V_H \geq 2.4$ V. What are the minimum W/L ratios of the NMOS and PMOS transistors required to meet these specifications? Assume $V_{DD} = 5$ V.

7.3 Dynamic Behavior of the CMOS Inverter

7.24. (a)What are the rise time, fall time, and average propagation delay for a symmetrical CMOS inverter with $(W/L)_N = 2/1$, $(W/L)_P = 5/1$, $V_{DD} = 2.5$ V, and $C = 0.20$ pF? (b) Repeat for $V_{DD} = 2.0$ V. (c) Repeat for $V_{DD} = 1.8$ V.

7.25. (a) Repeat problem 7.24(a) if the inverter is asymmetrical with $V_{TN} = 0.65$ V and $V_{TP} = -0.55$ V. What is the switching threshold v_I (where does $v_O = v_I$)? (b) Repeat for $V_{DD} = 1.8$ V. (c) Repeat for $V_{DD} = 3.3$ V.

7.26. (a) Repeat problem 7.24(a) if the inverter is asymmetrical with $V_{TN} = 0.55$ V and $V_{TP} = -0.65$ V. What is the switching threshold v_I (where does $v_O = v_I$)? (b) Repeat for $V_{DD} = 1.8$ V. (c) Repeat for $V_{DD} = 3.3$ V.

7.27. What are the rise time, fall time, and average propagation delay for a minimum size CMOS inverter in which both W/L ratios are 2/1? Assume a load capacitance of 0.4 pF and $V_{DD} = 2.5$ V.

7.28. Repeat problem 7.27 if $V_{TN} = 0.65$ V and $V_{TP} = -0.55$ V. What is the switching threshold $v_I (v_O = v_I)$ of the inverter?

7.29. What are the rise time, fall time, and average propagation delay for a symmetrical CMOS inverter with $(W/L)_N = 2/1$, $(W/L)_P = 5/1$, $C = 0.20$ pF, $V_{DD} = 3.3$ V, $V_{TN} = 0.75$ V, and $V_{TP} = -0.75$ V?

7.30. What are the rise time, fall time, and average propagation delay for a symmetrical CMOS inverter with $(W/L)_N = 2/1$, $(W/L)_P = 5/1$, $C = 0.15$ pF, $V_{DD} = 2.5$ V, $V_{TN} = 0.60$ V, and $V_{TP} = -0.60$ V?

7.31. What are the sizes of the transistors in the CMOS inverter if it must drive a 1-pF capacitance with an average propagation delay of 3 ns? Design the inverter for equal rise and fall times. Use $V_{DD} = 2.5$ V, $V_{TN} = 0.6$ V, $V_{TP} = -0.6$ V.

7.32. Design an asymmetrical inverter to meet the delay specification in Prob. 7.31 with $(W/L)_P = (W/L)_N$.

7.33. Design a symmetrical CMOS reference inverter to provide a delay of 1 ns when driving a 10-pF load. (a) Assume $V_{DD} = 2.5$ V. (b) Assume $V_{DD} = 3.3$ V and $V_{TN} = -V_{TP} = 0.75$ V.

7.34. Design an asymmetrical inverter to meet the delay specification in Prob. 7.33 with $(W/L)_P = 2(W/L)_N$.

7.35. Design a symmetrical CMOS reference inverter to provide a propagation delay of 200 ps for a load capacitance of 100 fF. Use $V_{DD} = 1.5$ V, $V_{TN} = 0.50$ V, and $V_{TP} = -0.50$ V.

7.36. Design an asymmetrical inverter to meet the delay specification in Prob. 7.35 with $(W/L)_P = (W/L)_N$.

7.37. Design a symmetrical CMOS reference inverter to provide a propagation delay of 400 ps for a load capacitance of 100 fF. Use $V_{DD} = 2.5$ V, $V_{TN} = 0.60$ V, and $V_{TP} = -0.60$ V.

7.38. Design an asymmetrical inverter to meet the delay specification in Prob. 7.37 with $(W/L)_P = (W/L)_N$.

7.39. (a) Scale the reference inverter in Fig. 7.12 to achieve a 0.4 ns delay with $C = 2$ pF. (b) What is the delay of the new inverter if $C = 3$ pF?

7.40. (a) Scale the reference inverter in Fig. 7.12 to achieve a 0.3 ns delay with $C = 0.5$ pF. (b) What is the delay of the new inverter if $C = 1.5$ pF?

*7.41. Use SPICE to determine the characteristics of the CMOS inverter for the design given in Fig. 7.12 if $C = 100$ fF. (a) Simulate the voltage transfer function. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input. What must be the total effective load capacitance C based on the propagation delay formula developed in the text?

**7.42. Use SPICE to simulate the behavior of a chain of five CMOS inverters similar to those in Fig. 7.13(b). The input to the first inverter should be a square wave with 0.1-ns rise and fall times and a period

of 100 ns. (a) Calculate t_r, t_f, τ_{PHL}, and τ_{PLH} using the input and output waveforms from the first inverter in the chain and compare your results to the formulas developed in the text. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} from the waveforms at the input and output of the fourth inverter in the chain, and compare your results to the formulas developed in the text. (c) Discuss the differences between the results in (a) and (b).

7.4 Power Dissipation and Power Delay Product in CMOS

7.43. A high-performance CMOS microprocessor design requires 500 million logic gates and will be placed in a package that can dissipate 100 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 1.8 V is used, what is the average current that must be supplied to the chip?

7.44. A certain packaged IC chip can dissipate 5 W. Suppose we have a CMOS IC design that must fit on one chip and requires 5 million logic gates. What is the average power that can be dissipated by each logic gate on the chip? If the average gate must switch at 5 MHz, what is the maximum capacitive load on a gate for $V_{DD} = 3.3$ V, 2.5 V and 1.8 V.

7.45. (a) The n-well in a CMOS process covers an area of 5 mm $\times$ 10 mm, and the saturation current density of the junction is 400 pA/cm^2. What is the total leakage current of the reverse-biased well? (b) Suppose the drain and source regions of the NMOS and PMOS transistors are each 0.5 μm $\times$ 1.25 μm in size, and the saturation current density of the junction is 150 pA/cm^2. If the chip has 200 million inverters, what is the total leakage current when $v_O = 2.5$ V? Assume $V_{DD} = 2.5$ V. (b) Repeat for $v_O = 0$ V.

7.46. A high-speed CMOS microprocessor has a 64-bit address bus and performs a memory access every 2 ns. Assume that all address bits change during every memory access and that each bus line represents a load of 25 pF. (a) How much power is being dissipated by the circuits that are driving these signals if the power supply is 2.5 V? (b) Repeat for 3.3 V.

*7.47. (a) A CMOS inverter has $(W/L)_N = 15/1$, $(W/L)_P = 15/1$, and $V_{DD} = 3.3$ V. What is the peak current in the logic gate and at what input voltage does it occur? (b) Repeat for $V_{DD} = 2.5$ V.

7.48. (a) Repeat Prob. 7.47(a) for $V_{DD} = 1.8$ V. (b) Repeat for $V_{DD} = 2.5$ V, $V_{TN} = 0.55$ V, and $V_{TP} = -0.65$ V.

*7.49. (a) A CMOS inverter has $(W/L)_N = 2/1$, $(W/L)_P = 5/1$, and $V_{DD} = 3.3$ V. Assume $V_{TN} = -V_{TP} = 0.7$ V. What is the peak current in the logic gate and at what input voltage does it occur? (b) Repeat for $V_{DD} = 2.0$ V with $V_{TN} = -V_{TP} = 0.5$ V.

7.50. (a) Repeat Prob. 7.49(a) for $V_{DD} = 2.0$ V, $V_{TN} = 0.45$ V, and $V_{TP} = -0.55$ V. (b) Repeat Prob. 7.49(a) for $V_{DD} = 2.0$ V, $V_{TN} = 0.55$ V, and $V_{TP} = -0.45$ V.

7.51. What is the power-delay product for the inverter in Prob. 7.24? How much power does the inverter dissipate if it is switching at a frequency of 100 MHz?

7.52. (a) What is the power-delay product for the inverter in Prob. 7.29? (b) Estimate the maximum switching frequency for this inverter. (c) How much power does the inverter dissipate if it is switching at the frequency found in (b)?

7.53. (a) What is the power-delay product for the inverter in Prob. 7.30? (b) Estimate the maximum switching frequency for this inverter. (c) How much power does the inverter dissipate if it is switching at the frequency found in (b)?

7.54. Plot the power-delay characteristic for the CMOS inverter family based on an inverter design in which $(W/L)_N = (W/L)_P$. Assume the load capacitance $C = 0.2$ pF. Use $V_{DD} = 2.5$ V and vary the power by changing the W/L ratios.

**7.55. Ideal constant-electric-field scaling of a MOS technology reduces all the dimensions and voltages by the same factor α. Assume that the capacitor C in Eq. (7.31) is proportional to the total gate capacitance of the MOS transistor: $C = C''_{ox} W/L$, and show that constant-field scaling results in a reduction of the PDP by a factor of α^3.

**7.56. For many years, MOS technology was scaled by reducing all the dimensions by the same factor α, but keeping the voltages constant. Assume that the capacitor C in Eq. (7.31) is proportional to the total gate capacitance of the MOS transistor: $C = C''_{ox} WL$, and show that this geometry scaling results in a reduction of the PDP by a factor of α.

**7.57. Use SPICE to simulate the behavior of a chain of five CMOS inverters with the same design as in Fig. 7.12 with $C = 0.25$ pF. The input to the first inverter should be a square wave with 0.1-ns rise

and fall times and a period of 30 ns. (a) Calculate t_r, t_f, τ_{PHL}, and τ_{PLH} using the input and output waveforms from the first inverter in the chain, and compare your results to the formulas developed in the text. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} from the waveforms at the input and output of the fourth inverter in the chain, and compare your results to the formulas developed in the text. (c) Discuss the differences between the results in (a) and (b).

**7.58. Use SPICE to simulate the behavior of a chain of five CMOS inverters with the same design as in Fig. 7.12 with $C = 1$ pF. The input to the first inverter should be a square wave with 0.1-ns rise and fall times and a period of 40 ns. (a) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} from the waveforms at the input and output of the fourth inverter in the chain, and compare your results to the formulas developed in the text. (b) Repeat the simulation for $(W/L)_P = (W/L)_N = 2/1$, and compare the results to those obtained in (a).

7.5 CMOS NOR and NAND Gates

7.59. (a) Draw the circuit schematic for a four-input NOR gate. What are the W/L ratios of the transistors based on the reference inverter design in Fig. 7.12? (b) What should be the W/L ratios if the NOR gate must drive twice the load capacitance with the same delay as the reference inverter?

7.60. Draw the circuit schematic of a four-input NOR gate. Suppose the PMOS transistors are chosen to have $(W/L)_P = 2/1$. What are the corresponding W/L ratios of the NMOS devices, if the gate is to have symmetrical delay characteristics?

7.61. Draw the circuit schematic of a three-input NOR gate. Suppose the PMOS transistors are chosen to have $(W/L)_P = 2/1$. What are the corresponding W/L ratios of the NMOS devices, if the gate is to have symmetrical delay characteristics?

7.62. (a) Draw the circuit schematic for a four-input NAND gate. What are the W/L ratios of the transistors based on the reference inverter design in Fig. 7.12? (b) What should be the W/L ratios if the NOR gate must drive three times the load capacitance with the same delay as the reference inverter?

7.63. Draw the circuit schematic of a four-input NAND gate. Suppose the NMOS transistors are chosen to have $(W/L)_N = 2/1$. What are the corresponding W/L ratios of the PMOS devices, if the gate is to have symmetrical delay characteristics?

7.64. Draw the circuit schematic of a three-input NAND gate. Suppose the NMOS transistors are chosen to have $(W/L)_N = 2/1$. What are the corresponding W/L ratios of the PMOS devices, if the gate is to have symmetrical delay characteristics?

7.65. Design a circuit to multiply two one-bit numbers. (*Hint:* Construct a truth table for output bit M based on two inputs A and B.) Choose the W/L ratios based on the inverter in Fig. 7.12.

**7.66. Use SPICE to determine the characteristics of the two-input CMOS NOR gate given in Fig. 7.19 with a load capacitance of 1 pF. Assume that $\gamma = 0$ for all transistors. (a) Simulate the voltage transfer function by varying the voltage at input A with the voltage at input B fixed at 2.5 V. (b) Repeat the simulation in (a) but now vary the voltage at input B with the voltage at input A fixed at 2.5 V. Plot the results from (a) and (b) and note any differences. (c) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input at input A with the voltage at input B fixed at 2.5 V. (d) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input at input B with the voltage at input A fixed at 2.5 V. (e) Compare the results from (c) and (d). (f) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a single square wave input applied to both inputs A and B. Compare the results to those in (c) and (d).

**7.67. Repeat (a) and (b), Prob. 7.66, using the nonzero values for the parameter γ from the device parameter tables.

**7.68. Use SPICE to determine the characteristics of the two-input CMOS NAND gate given in Fig. 7.23 with a load capacitance of 1 pF. Assume that $\gamma = 0$ for all transistors. (a) Simulate the voltage transfer function by varying the voltage at input A with the voltage at input B fixed at 2.5 V. (b) Repeat the simulation in (a) but now vary the voltage at input B with the voltage at input A fixed at 2.5 V. Plot the results from (a) and (b) and note any differences. (c) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input at input A with the voltage at input B fixed at 2.5 V. (d) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input at input B with the voltage at input A fixed at 2.5 V. (e) Compare the results from (c) and (d). (f) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a single square wave input applied to both inputs A and B. Compare the results to those in (c) and (d).

**7.69. Repeat (a) and (b), Prob. 7.68, using the nonzero values for the parameter γ from the device parameter tables.

7.6 Design of Complex Gates in CMOS

7.70. What are the worst case rise and fall times and average propagation delays of the CMOS gate in Fig. 7.26(b) for a load capacitance of 1.25 pF?

7.71 (a) What is the equivalent W/L ratio of the NMOS switching network in Fig. 7.26(b) when all of the NMOS transistors are on? (b) Repeat for the PMOS network.

**7.72. (a) How many transistors are needed to implement the CMOS gate in Fig. 7.29 using depletion-mode NMOS? (b) Compare the total gate area of the CMOS and NMOS designs if they are both designed for a 10-ns average propagation delay for a load capacitance of 1 pF.

7.73. (a) What is the logic function implemented by the gate in Fig. P7.73? (b) Design the PMOS transistor network. Select the device sizes for both the NMOS and PMOS transistors to give a delay similar to that of the CMOS reference inverter. C is the same. (c) What is the equivalent W/L ratio of the NMOS switching network when all of the NMOS transistors are on? (d) Repeat for the PMOS network.

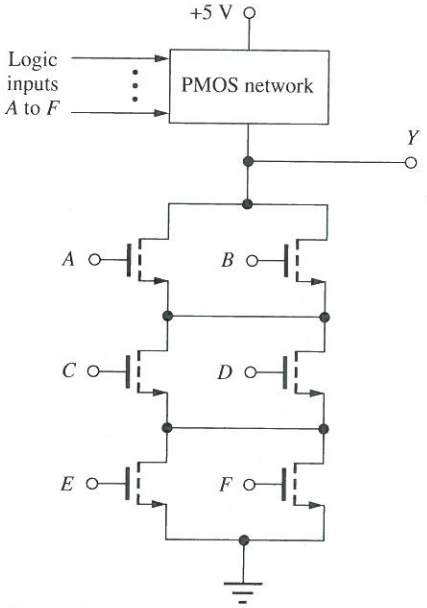


Figure P7.73

7.74. (a) What is the logic function implemented by the gate in Fig. P7.74? (b) Design the PMOS transistor network. Select the device sizes for both the NMOS and PMOS transistors to give a delay of approximately one-half the delay of the CMOS reference inverter. C is the same. (c) What is the equivalent W/L ratio of the NMOS switching network when all of the NMOS transistors are on? (d) Repeat for the PMOS network.

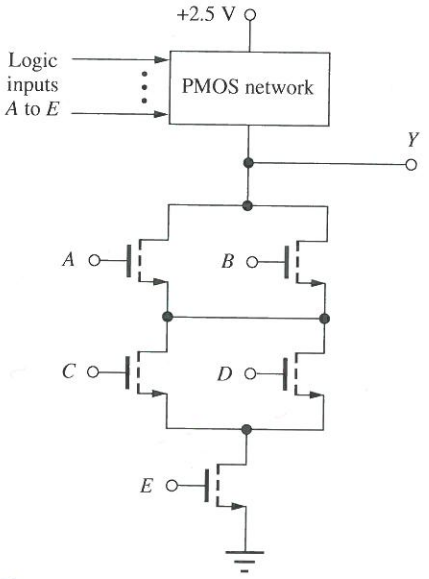


Figure P7.74

7.75. (a) What is the logic function implemented by the gate in Fig. P7.75? (b) Design the PMOS transistor network. Select the device sizes for both the NMOS

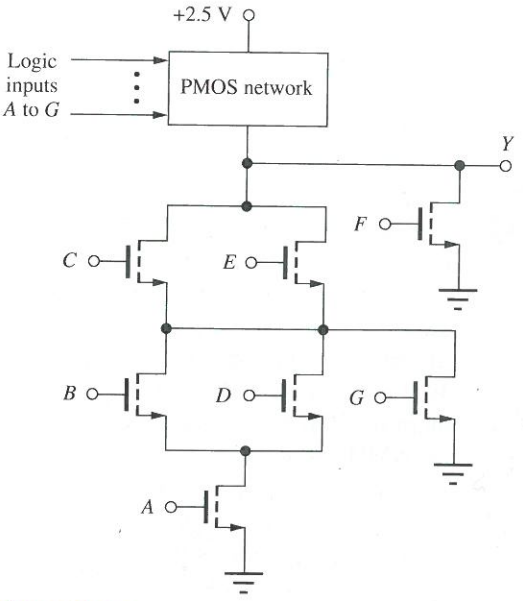


Figure P7.75

and PMOS transistors to give a delay of approximately one-half the delay of the CMOS reference inverter. C is the same. (c) What is the equivalent W/L ratio of the NMOS switching network when all of the NMOS transistors are on? (d) Repeat for the PMOS network.

7.76. (a) What is the logic function implemented by the gate in Fig. P7.76? (b) Design the NMOS transistor network. Select the device sizes for both the NMOS and PMOS transistors to give a delay similar to that of the CMOS reference inverter. C is the same. (c) What is the equivalent W/L ratio of the PMOS switching network when all of the PMOS transistors are on? (d) Repeat for the NMOS network.

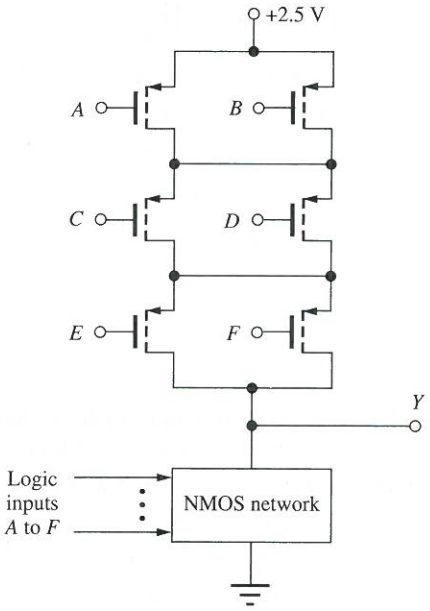


Figure P7.76

7.77. (a) What is the logic function implemented by the gate in Fig. P7.77? (b) Design the NMOS transistor network. Select the device sizes for both the NMOS and PMOS transistors to give a delay of approximately one-fourth the delay of the CMOS reference inverter. C is the same. (c) What is the equivalent W/L ratio of the PMOS switching network when all of the PMOS transistors are on? (d) Repeat for the NMOS network.

7.78. Draw the logic diagram and transistor implementation for a (2-3-1) AOI gate. Use the graphical approach to design the PMOS network. Choose the size of the transistors based upon the reference inverter in Fig. 7.12.

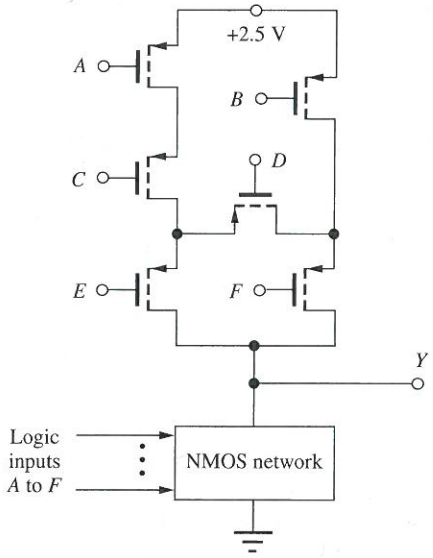


Figure P7.77

7.79. Draw the logic diagram and transistor implementation for a (3-2-3-1) AOI gate. Use the graphical approach to design the PMOS network. Choose the size of the transistors based upon the reference inverter in Fig. 7.12.

7.80. (a) Draw the NMOS and PMOS graphs for the (2-2-1) AOI in the Electronics in Action figure on page 394. (b) Find an Euler path for this circuit if it exists. (c) Draw the NMOS and PMOS graphs for a (2-2-2) AOI. (d) Find an Euler path for part (d) if it exists.

7.81. Redraw Fig. 7.28 and highlight the conducting path(s) for the following sets of inputs for ABCDE: (a) 10011, (b) 10001, (c) 11101, (d) 00010.

7.82. Draw the circuit for Prob. 7.73 and highlight the conducting path(s) for the following sets of inputs for ABCDEF: (a) 100110, (b) 011001, (c) 010101, (d) 110011.

7.83. Design a CMOS logic gate that implements the logic function $Y = \overline{A(BC + DE)}$ and is twice as fast as the CMOS reference inverter when loaded by a capacitance of $2C$.

7.84. Design a CMOS logic gate that implements the logic function $Y = \overline{ABC + DE}$, based on the CMOS reference inverter. Select the transistor sizes to give the same delay as that of the reference inverter if the load capacitance is the same as that of the reference inverter.

7.85. Design a CMOS logic gate that implements the logic function $Y = \overline{A(B + CD) + E}$ and has the same logic delay as the CMOS reference inverter when driving a capacitance of $4C$.

7.86. Design a CMOS logic gate that implements the logic function $Y = \overline{A(B + C(D + E))}$, based on the CMOS reference inverter. Select the transistor sizes to give the same delay as that of the reference inverter if the load capacitance is the same as that of the reference inverter.

7.87. Design a complex gate implementation of a one-bit half adder for which the sum bit is described by $S = X \oplus Y$, and the carry bit is given by $C = A \cdot B$. Choose the W/L ratios based on the reference inverter design in Fig. 7.12. Assume that true and complement values of each variable are available as inputs. (*Note:* Two gate designs are needed, one for S and one for C.)

7.88. Design a complex gate implementation of a 1-bit full adder for which the ith sum bit is described by $S_i = X_i \oplus Y_i \oplus C_{i-1}$, and the ith carry bit is given by $C_i = X_i \cdot Y_i + X_i \cdot C_{i-1} + Y_i \cdot C_{i-1}$. Choose the W/L ratios based upon the reference inverter design in Fig. 7.12. Assume that true and complement values of each variable are available as inputs. (*Note:* Two gate designs are needed, one for S_i and one for C_i.)

7.89. Design a complex gate implementation of a 2-bit parallel multiplier. [*Note:* The circuit should produce a 4-bit output (e.g., $11_2 \times 11_2 = 1001_2$), and a separate circuit should be designed for each output bit.] Choose the W/L ratios based on the inverter in Fig. 7.12.

7.7 Minimum Size Gate Design and Performance

7.90. The five-input NAND gate in Fig. 7.24 is implemented with transistors all having $W/L = 2/1$. What is the propagation delay for this gate for a load capacitance $C = 180$ fF? Assume $V_{DD} = 2.5$ V. What would be the delay of the reference inverter for $C = 180$ fF?

7.91. The three-input NOR gate in Fig. 7.21 is implemented with transistors all having $W/L = 2/1$. What is the propagation delay for this gate for a load capacitance $C = 400$ fF? Assume $V_{DD} = 2.5$ V. What would be the delay of the reference inverter for $C = 400$ fF?

7.92. A (2-3-1) AOI is implemented with transistors all having $W/L = 2/1$. What are the worst-case values of τ_{PLH} and τ_{PHL} if $V_{DD} = 2.5$ V and $C = 350$ fF?

7.93. A (2-2-2) AOI is implemented with transistors all having $W/L = 2/1$. What are the worst-case values of τ_{PLH} and τ_{PHL} if $V_{DD} = 2.5$ V and $C = 200$ fF?

7.94. What are the worst-case values of τ_{PHL} and τ_{PLH} for the gate in Fig. 7.28 when it is implemented using only 2/1 transistors and drives a load capacitance of 0.5 pF? Assume $V_{DD} = 2.5$ V.

7.95. What is the worst-case value of τ_{PHL} for the gate in Fig. P7.73 when it is implemented using only 2/1 transistors and drives a load capacitance of 0.5 pF? Assume $V_{DD} = 2.5$ V.

7.96. (a) Use a transient simulation in SPICE to find the average propagation delay of a cascade connection of 10 minimum size inverters ($W/L = 2/1$) in series. Assume each has a capacitive load C of 200 fF and $V_{DD} = 2.5$ V. (b) Repeat for a cascade of 10 symmetrical reference inverters with the same design as in Fig. 7.12, and compare the average propagation delays.

7.8 Dynamic Domino CMOS Logic

7.97. (a) Draw the circuit schematic for a two-input domino CMOS NOR gate. Assume that true and complement values of each variable are available as inputs. (b) Repeat for a two-input domino CMOS NAND gate.

7.98. (a) Draw the circuit schematic for a two-input domino CMOS OR gate. Assume that true and complement values of each variable are available as inputs. (b) Repeat for a two-input domino CMOS AND gate.

7.99. (a) Draw the circuit schematic for a three-input domino CMOS NOR gate. Assume that true and complement values of each variable are available as inputs. (b) Repeat for a three-input domino CMOS NAND gate.

7.100. (a) Draw the circuit schematic for a three-input domino CMOS OR gate. Assume that true and complement values of each variable are available as inputs. (b) Repeat for a three-input domino CMOS AND gate.

7.101. Draw the circuit schematic for a (2-2-2) AOI in domino CMOS.

7.102. Draw the circuit schematic for a (3-2-1) AOI in domino CMOS.

*7.103. (a) Suppose that inputs A_0, A_1, and A_2 are all 0 in the domino CMOS gate in Fig. P7.103, and the clock has just changed to the evaluate phase. If A_0 now changes to a 1, what happens to the voltage at node B if $C_1 = 2C_2$? (*Hint:* Charge sharing occurs between C_1 & C_2.) (b) Now A_1 changes to a 1. What happens to the voltage at node B if $C_3 = C_2$? (c) If the output inverter is a symmetrical design, what is the minimum ratio of C_1/C_2 (assume $C_3 = C_2$) for which the gate maintains a valid output? $V_{DD} = 2.5$ V

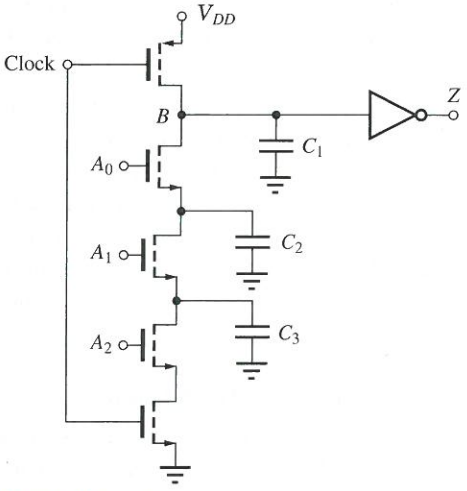


Figure P7.103

7.104. Draw the mirror image of the gate in Fig. P7.102 by replacing NMOS transistors with PMOS transistors and vice versa. Assume the logic inputs remain the same and write an expression for the logic function Z.

7.105. Draw the circuit schematic for a domino CMOS gate that implements the sum of products (SOP) logic function $Z = AB + CD$. Assume that true and complement values of each variable are available as inputs.

7.106. Draw the circuit schematic for a domino CMOS gate that implements the product of sums (POS) logic function $Z = (A + B)(C + D)$. Assume that true and complement values of each variable are available as inputs.

7.107. Draw the circuit schematic for a domino CMOS gate that implements the sum-of-products (SOP) logic function $Z = AB + CD + EF$. Assume that true and complement values of each variable are available as inputs. (Remember DeMorgan's theorem.)

7.108. Draw the circuit schematic for a domino CMOS gate that implements the product-of-sums (POS) logic function $Z = (A + B)(C + D)(E + F)$. Assume that true and complement values of each variable are available as inputs. (Remember DeMorgan's theorem.)

7.9 Cascade Buffers

7.109. Design an optimized cascade buffer to drive a load capacitance of $5000C_o$. (a) What is the optimum number of stages? (b) What are the relative sizes of each inverter in the chain (see Fig. 7.33)? (c) What is the delay of the buffer in terms of τ_o?

7.110. Design an optimized cascade buffer to drive a load capacitance of 10 pF if the capacitance of the symmetrical reference inverter is 80 fF. What is the optimum number of stages? What are the relative sizes of each inverter in the chain? What is the total delay of the buffer for $V_{DD} = 2.5$ V?

7.111. Design an optimized cascade buffer to drive a load capacitance of 40 pF if the capacitance of a symmetrical reference inverter is 50 fF. What is the optimum number of stages? What are the relative sizes of each inverter in the chain? What is the total delay of the buffer for $V_{DD} = 2.5$ V?

**7.112. Assume that the area of each inverter in a cascade buffer is proportional to the taper factor β and that the unit size inverter has as area A_o. Write an expression for the total area of an N-stage cascade buffer. In the example in Fig. 7.34, buffers with $N = 6$ and $N = 7$ have approximately the same delay. Compare the area of these two buffer designs using your formula.

7.10 The CMOS Transmission Gate

7.113. (a) Calculate the on-resistance of an NMOS transistor with $W/L = 20/1$ for $V_{GS} = 2.5$ V, $V_{SB} = 0$ V, and $V_{DS} = 0$ V. (b) Calculate the on-resistance of a PMOS transistor with $W/L = 20/1$ for $V_{SG} = 2.5$ V, $V_{SB} = 0$ V, and $V_{SD} = 0$ V. (c) What do we mean when we say that a transistor is "on" even though I_D and $V_{DS} = 0$?

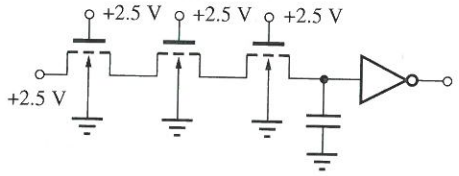
7.114. Calculate the maximum and minimum values of the equivalent on-resistance for the transmission gate in Fig. 7.36.

7.115. (a) What is the largest value of the on-resistance of a transmission gate with $W/L = 10/1$ for both transistors if the input voltage range is $0 \leq v_I \leq 1$ V and the power supply is 2.5 V? At what input

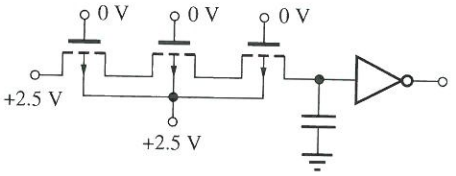
voltage does it occur? (b) Repeat for $0 \leq v_I \leq 2.5$ V.

7.116. A certain analog multiplexer application requires the equivalent on-resistance R_{EQ} of a transmission gate to always be less than 250 Ω for $0 \leq v_I \leq 2.5$ V. What are the minimum values of W/L for the NMOS and PMOS transistors if $V_{TON} = 0.75$ V, $V_{TOP} = -0.75$ V, $\gamma = 0.5\sqrt{\text{V}}$, $2\phi_F = 0.6$ V, $K'_p = 40\ \mu\text{A/V}^2$, and $K'_n = 100\ \mu\text{A/V}^2$?

7.117. (a) What are the voltages at the nodes in the pass-transistor networks in Fig. P7.117. For NMOS transistors, use $V_{TO} = 0.70$ V, $\gamma = 0.6\sqrt{\text{V}}$, and $2\phi_F = 0.6$ V. For PMOS transistors, $V_{TO} = -0.70$ V and $\gamma = 0.5\sqrt{V}$. (b) What would be the voltages if transmission gates were used in place of each transistor?



(a)



(b)

Figure P7.117

7.11 CMOS Latchup

7.118. Simulate CMOS latchup using the circuit in Fig. 7.37(b) and plot graphs of the voltages at nodes 2, 3, and 4 as well as the current supplied by V_{DD}. Discuss the behavior of the voltages and identify important voltage levels, current levels, and slopes on the graphs.

7.119. Repeat Prob. 7.118 if the values of R_n and R_p are reduced by a factor of 10.

7.120. Draw the cross section and equivalent circuit, similar to Fig. 7.37, for a p-well CMOS technology.

Additional Problems

7.121. (a) Verify Eq. (7.9). (b) Verify Eq. (7.13).

**7.122. (a) Calculate the sensitivity $S_{K_n}^{\tau_p} = (K_n/\tau_p)(d\tau_p/dK_n)$ of the propagation delay τ_p in Eq. (7.18) to changes in K_n. If the IC processing causes K_n to be 25 percent below its nominal value, what will be the percentage change in τ_p? (b) Calculate the sensitivity $S_{V_{TN}}^{\tau_p} = (V_{TN}/\tau_p)(d\tau_p/dV_{TN})$ of the propagation delay τ_p in Eq. (7.18) to changes in V_{TN}. If the IC processing causes V_{TN} to change from a nominal value of 0.75 V to 0.85 V, what will be the percentage change in τ_p?

7.123. Calculate logic delay versus input signal rise time for a minimum size inverter with a load capacitance of 1 pF for $0.1\ \text{ns} \leq t_r \leq 5$ ns.

7.124. An NMOS transistor is to be used as a power switch to disable one core of a multicore processor chip that operates from a 2.5 V power supply. When the core is enabled, its current is 4 A. What is the W/L ratio of the NMOS transistor if the voltage drop across the transistor must be less than 100 mV? If $L = 1\ \mu$m, estimate the area of the transistor.

7.125. CMOS with a PDP of 50 fJ is to be used in a chip design that requires 100 million gates. The chip will be placed in a package that can safely dissipate 40 W. What is the minimum logic gate delay that can be used in the design if all the gates operate at the same speed and 20 percent of the gates are switching at any given time?