3. W. M. Regitz and J. A. Karp, "A three-transistor cell, 1024-bit, 500 ns MOS RAM," *ISSCC Digest of Technical Papers,* pp. 36–39, February 1970.

4. *Digest of the IEEE International Electron Devices Meeting* (IEDM), December of each year.

5. Robert H. Dennard; patent 3,387,286 assigned to the IBM Corporation.

6. H. C. Lin and L. W. Linholm, "An optimized output stage for MOS integrated circuits," *IEEE JSSC,* vol. SC-10, pp. 106–109, April 1975.

7. R. C. Jaeger, "Comments on 'An optimized output stage for MOS integrated circuits,'" *IEEE JSSC,* vol. SC-10, pp. 185–186, June 1975.

8. Mikio Asakura et al., "A 34 ns 256 Mb DRAM with boosted sense-ground scheme," *ISSCC Digest of Technical Papers,* pp. 140–141, 324, February 1994.

9. *Digest of the IEEE Custom Integrated Circuits Conference,* April of each year.

10. *Digests of the Symposium on VLSI Circuits and the Symposium on VLSI Technology,* June of each year.

11. *IEEE Journal of Solid-State Circuits,* monthly.

12. *IEEE Transactions on Electron Devices,* monthly.

13. Carver Mead and Lynn Conway, *Introduction to VLSI Systems,* Addison-Wesley, Reading, MA: 1980.

14. R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," *IEEE Journal of Solid-State Circuits,* vol. SC-7, no. 2, pp. 146–152, April 1972.

15. J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration," *IEEE Journal of Solid-State Circuits,* vol. SC-35, no. 10, pp. 1515–1516, October 2000.

16. J. R. Houser, "Noise margin criteria for digital logic circuits," *IEEE Trans. on Education,* vol. 36, no. 4, pp. 363–368, November 1993.

17. J. Lohstroh, E. Seevinck, and J. Degroot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE Journal of Solid-State Circuits,* vol. SC-18, no. 6, pp. 803–806, December 1983.

PROBLEMS

Unless otherwise specified, use $K'_n = 100 \ \mu A/V^2$, $K'_p = 40 \ \mu A/V^2$, $V_{TON} = 0.7$ V, $V_{TOP} = -0.7$ V, $\gamma = 0.5 \ \sqrt{V}$, $2\phi_F = 0.6$ V. For simulation, use the models in Appendix B.

8.1 Random-Access Memory (RAM)

8.1. (a) How many bits are actually in a 256-Mb memory chip? In a 1-Gb chip? (b) How many 128-Kb blocks must be replicated to form the 256-Mb memory in Fig. 8.1?

8.2. How much leakage is permitted per memory cell in a 256-Mb static CMOS memory chip if the total standby current of the memory is to be less than 1 mA? (b) Repeat for a 4-Gb memory.

8.3. Suppose a memory chip has a 128-bit-wide external memory bus. What is the power dissipated driving the memory bus at a 1-GHz data rate if each bus line has 10 pF of capacitance, and the voltage is 1.8 V? (b) Repeat for 3 GHz and 1.8 V.

8.4. Suppose that each cell in a 1-Gbit memory chip must be refreshed every 10 ms. What is the power dissipated in refreshing the chip if the cell capacitance is 100 fF and the cell voltage is 2.5 V? Assume that 50 percent of the cells have 1 bits stored and that the cell voltage is completely discharged and restored during the refresh operation.

8.2 Static Memory Cells

8.5. Find the voltages corresponding to D and $\overline{D}$ in an NMOS memory cell with resistor loads in place of the PMOS transistors in Fig. 8.6 if $R = 10^{10} \ \Omega$, $V_{DD} = 3$ V, and $W/L = 2/1$. Use $V_{TO} = 0.75$ V, $\gamma = 0.5 \ \sqrt{V}$, and $2\phi_F = 0.6$ V.

*8.6. Assume that the two bitlines are fixed at 1.5 V in the circuit in Figs. 8.7 and 8.8 and that a steady-state

condition has been reached, with the wordline voltage equal to 3 V. Assume that the inverter transistors all have $W/L = 1/1$, $V_{TN} = 0.7$ V, $V_{TP} = -0.7$ V, and $\gamma = 0$. What is the largest value of W/L for M_{A1} and M_{A2} (use the same value) that will ensure that the voltage at $D_1 \leq 0.7$ V and the voltage at $D_2 \geq 2.3$ V?

*8.7. Simulate the response time of the 6-T cell in Fig. 8.6 from an initial condition of $D_1 = 1.55$ V and $D_2 = 1.45$ V with the access transistors off. How long does it take for the cell voltages to reach 90 percent of their final values? Use $V_{DD} = 3$ V and a symmetrical cell design, with W/L of the NMOS transistors $= 2/1$. Use the SPICE models from Appendix B.

8.8. Simulate and plot a graph of the transients that occur when writing a 0 into a cell containing a 0, as in Fig. 8.12. Discuss the results.

8.3 Dynamic Memory Cells

8.9. The 1-T cell in Fig. P8.9 uses a bitline voltage of 2.5 V and a wordline voltage of 2.5 V. (a) What are the cell voltages stored on C_C for a 1 and 0 if $V_{TO} = 0.6$ V, $\gamma = 0.5 \sqrt{V}$, and $2\phi_F = 0.6$ V? (b) What would be the minimum wordline voltage needed in order for the cell voltage to reach 2.5 V for a 1?
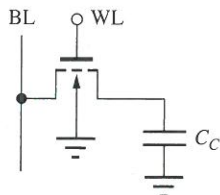

Figure P8.9

8.10. Repeat Prob. 8.9 if the bitline and wordline voltages are 1.8 V.

8.11. Substrate leakage currents usually tend to destroy only one of the two possible states in the 1-T cell. For the circuit in Fig. P8.9, which level is the most sensitive to leakage currents and why?

8.12. Find an expression for the energy that is lost during the charge redistribution for reading out the data in the 1-T? (a) How much energy is lost if $V_C = 1.9$ V, $V_{BL} = 1$ V, and $C_C = 25$ fF. State your assumptions. (b) Suppose a 128 Mb memory using these cells is refreshed every 5 ms. What is the average power consumed by the charge redistribution operation?

*8.13. The gate-source and drain-source capacitances of the MOSFET in Fig. P8.9 are each 100 fF, and $C_C = 75$ fF. The bitline and wordline have been stable at 2.5 V for a long time. The wordline signal is shown in Fig. P8.13. What is the voltage stored on C_C before the wordline drops? Estimate the drop in voltage on the C_C due to coupling of the wordline signal through the gate-source capacitance. Use $V_{TO} = 0.70$ V, $\gamma = 0.5 \sqrt{V}$, and $2\phi_F = 0.6$ V.
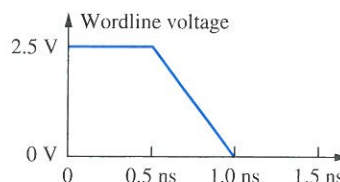

Figure P8.13

8.14. A 1-T cell has $C_C = 60$ fF and $C_{BL} = 7.5$ pF. (a) If the bitlines are precharged to 2.5 V, and the cell voltage is 0 V, what is the change in bitline voltage ΔV following cell access? (b) What is the final voltage in the cell?

8.15. A 1-T cell memory can be fabricated using PMOS transistors in the array shown in Fig. P8.15. (a) What are the voltages stored on the capacitor corresponding to logic 0 and 1 levels for a technology using $V_{DD} = 3.3$ V? (b) Repeat for $V_{DD} = 2.5$ V.
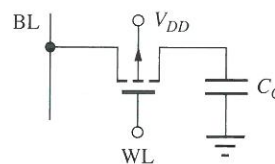

Figure P8.15

8.16. The bottom electrode of the storage capacitor in the 1-T cell is often connected to a voltage V_{PP} rather than ground, as shown in Fig. P8.16. Suppose that $V_{PP} = 5$ V. (a) What are the voltages stored in the cell at node V_C for $0 = 0$ V on the bitline and $1 = 3$ V on the bitline? Assume the wordline can be driven to 3 V. (b) Which level will deteriorate due to leakage in this cell?
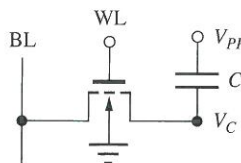

Figure P8.16

8.17. (a) Calculate the cell voltage for the boosted word-line version of the 1-T cell in Fig. 8.24 and show that the value in the text is correct. (b) Verify that the value of the current entering the sense amplifier node from the 1-T cell immediately following activation of the wordline is 216 µA.

*8.18. The 1-T cell in Fig. P8.18 uses bitline and wordline voltages of 0 V and 5 V. (a) What are the cell voltages stored on C_C for a 1 and 0 if $V_{TO} = -0.80$ V, $\gamma = 0.65$ V$^{0.5}$, and $2\phi_F = 0.6$ V? (b) What would be the minimum wordline voltage needed for the stored cell voltage to reach 0 V for a 0 state?
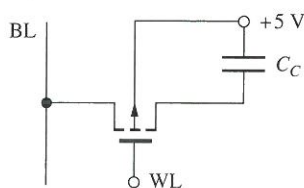
Figure P8.18

*8.19. In the discussion of the 1-T cell in the text, an improvement factor of 15 was stated for current drive from the boosted wordline cell compared to the normal cell. How much of this factor of 15 is attributable to the increased V_{DS} across the access transistor, and what portion is attributable to the increased gate voltage?

8.20. Simulate the refresh operation of the 4-T dynamic cell in Fig. P8.20. For initial conditions, assume that node D has decreased to 1 V, and node $\overline{D}$ is at 0 V. Use $BL = 3$ V, $\overline{BL} = 3$ V, $W/L = 2/1$ for all transistors, and the bitline capacitance is 500 fF.
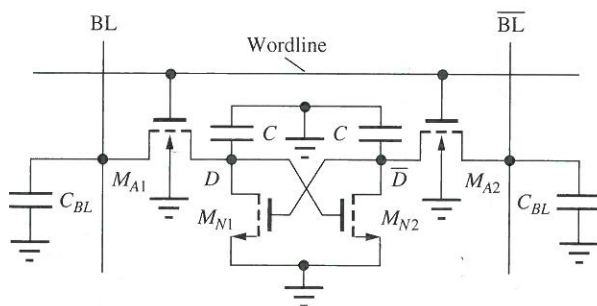

Figure P8.20

**8.21. Simulate the read access operation of the 4-T cell in Fig. P8.21 and discuss the waveforms that you obtain. What is the access time of the cell from the time the wordline is activated until the data is valid at the output of the sense amplifier? Use $W/L = 2/1$ for all devices, and assume $C_{BL} = 1$ pF, with $V_{DD} = 3$ V.
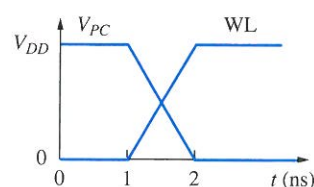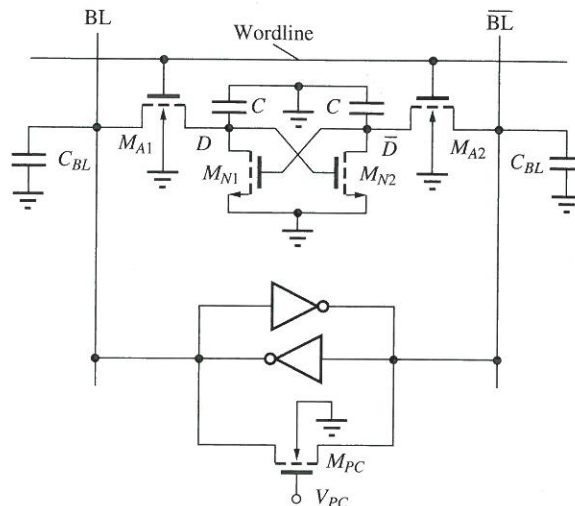

Figure P8.21

8.4 Sense Amplifiers

8.22. A simple CMOS sense amplifier is shown in Fig. P8.22. Suppose $V_{DD} = 2.5$ V and the W/L ratios of all the NMOS and PMOS transistors are 5/1 and 10/1, respectively. What is the total current through the sense amplifier when the precharge transistor is on? How much power will be consumed by 1024 of these sense amplifiers operating simultaneously?
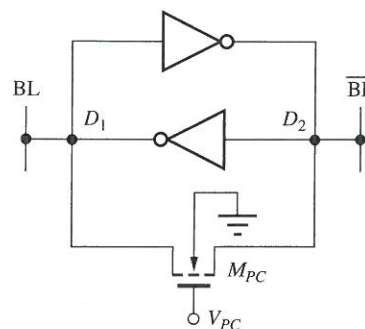

Figure P8.22

**8.23. The two bitlines in Fig. 8.29 are driven above V_{DD} by capacitive coupling of the precharge signal through the gate capacitance of the precharge devices. (a) Calculate the expected voltage change ΔV on the bitlines due to this coupling and compare to the simulation results in the figure. (b) What is the largest possible value of ΔV? See Appendix B for transistor models. Use $C_{BL} = 500$ fF.

**8.24. A transient drop can be observed in the waveforms for the two bitlines in Fig. 8.25 due to capacitive coupling of the precharge signal through the gate capacitance of the precharge device. Calculate the expected voltage change ΔV on the bitlines due to this coupling and compare to the simulation results in the figure. The BL capacitances are each 500 fF. See Appendix B for transistor models.

**8.25. Figure P8.25 shows the basic form of a charge-transfer sense amplifier that can be used for amplifying the output of a 1-T cell. Assume that the switch closes at $t = 0$, that capacitor C_C is initially discharged, and that C_L is initially charged to $+3$ V. Also assume that charge sharing between C_C and C_{BL} occurs instantaneously. Find the total change in the output voltage Δv_O that occurs once the circuit returns to steady-state conditions following the switch closure. Assume $C_C = 50$ fF, $C_{BL} = 1$ pF, $C_L = 100$ fF, and $W/L = 50/1$. (*Hint:* The MOSFET will restore the BL potential to the original value, and the total charge that flows out of the source of the FET must be supplied from the drain.)
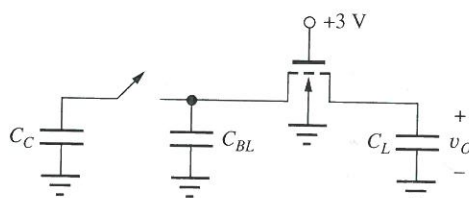

Figure P8.25   Charge transfer sense amplifier.

8.26. Simulate the circuit in Fig. P8.25 using a MOSFET ($W/L = 4/1$) for the switch and compare the results to your hand calculations.

**8.27. Convince yourself of the statement that any voltage imbalance in the cross-coupled latch will be reinforced by simulating the CMOS latch of Fig. P8.27 using the following initial conditions: (a) $D_1 = 1.45$ V and $D_2 = 1.55$ V, (b) $D_1 = 1$ V and $D_2 = 1.25$ V, (c) $D_1 = 2.75$ V and $D_2 = 2.70$ V.

Assume all W/L ratios are 2/1 and $V_{DD} = 3.3$ V, and use bitline capacitances of 1 pF.
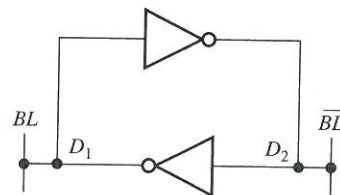

Figure P8.27

*8.28. The W/L ratios of the NMOS and PMOS transistors are 2/1 and 4/1, respectively, in the CMOS inverters in Fig. P8.28. The bitline capacitances are 400 fF, W/L of M_{PC} is 10/1, and $V_{DD} = 3$ V. (a) Simulate the switching behavior of the symmetrical latch and explain the behavior of the voltages at nodes D_1 and D_2. (b) Now suppose that a design error occurred and the W/L ratio of M_{N2} is 2.2/1 instead of 2/1. Simulate the latch again and explain any changes in the behavior of the voltages at nodes D_1 and D_2.
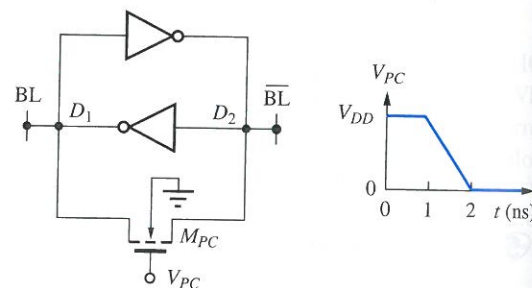

Figure P8.28

*8.29. Simulate the response of the NMOS clocked sense amplifier in Fig. P8.29 if $V_{DD} = 3$ V. What are the final voltage values on the two bitlines? How long does it take the sense amplifier to develop a
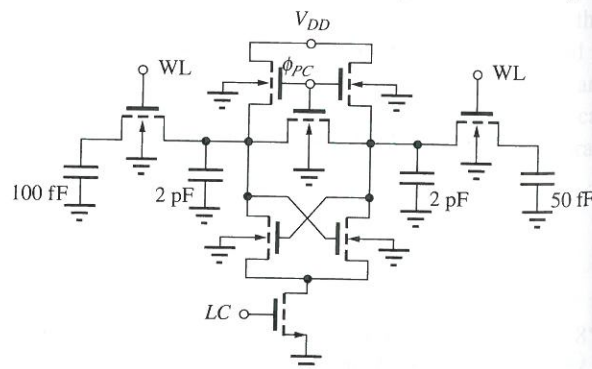

Figure P8.29

difference of 1.5 V between the two bitlines? Assume that all clock signals have amplitudes equal to V_{DD} and rise or fall times of 1 ns. Assume that the three signals are delayed successively by 0.5 ns in a manner similar to Fig. 8.29.

*8.30. Repeat Prob. 8.29 for $V_{DD} = 5$ V.

8.31. Simulate the transfer function of two cascaded CMOS inverters with all 2/1 devices and find the three equilibrium points. Use $V_{DD} = 3$ V.

8.32. (a) Find the noise margins for a memory cell formed from two cross-coupled inverters as defined in Prob. 8.31. Use the method described in the EIA on page 420. (b) Repeat for a symmetrical inverter using a 2/1 NMOS device and a 5/1 PMOS device.

8.5 Address Decoders

8.33. Calculate the number of transistors required to implement a 7-bit column decoder using (a) NMOS pass-transistor logic and (b) standard NOR logic.

8.34. (a) How many transistors are required to implement a full 12-bit NOR address decoder similar to that of Fig. 8.30? (b) How many transistors are required to implement a full 12-bit NAND address decoder similar to that of Fig. 8.31?
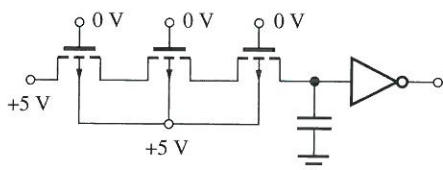
8.35. Draw the schematic of a 3-bit OR address decoder using domino CMOS.

8.36. What are the voltages at the nodes in the pass-transistor networks in Fig. P8.36? For NMOS transistors, use $V_{TO} = 0.8$ V, $\gamma = 0.6 \sqrt{V}$, and $2\phi_F = 0.6$ V. For PMOS transistors, $V_{TO} = -0.8$ V and $\gamma = 0.6\sqrt{V}$.
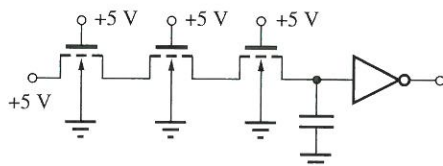
(a)

(b)

Figure P8.36

*8.37. (a) Suppose that inputs A_0, A_1, and A_2 are all 0 in the domino CMOS gate in Fig. P8.37, and the clock has just changed to the evaluate phase. If A_0 now changes to a 1, what happens to the voltage at node B if $C_1 = 2C_2$? (*Hint:* Remember the charge-sharing phenomenon.) (b) Now A_1 changes to a 1—what happens to the voltage at node B if $C_3 = C_2$? (c) If the output inverter is a symmetrical design, what is the minimum ratio of C_1/C_2 (assume $C_3 = C_2$) for which the gate maintains a valid output? Assume $V_{DD} = 5$ V.
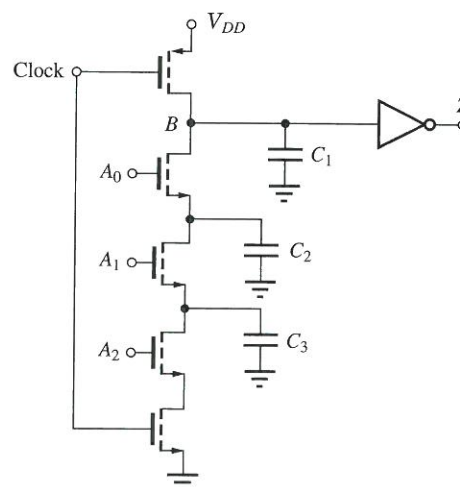

Figure P8.37

8.38. Draw the mirror image of the gate in Fig. P8.37 by replacing NMOS transistors with PMOS transistors and vice versa. Assume the logic inputs remain the same and write an expression for the logic function Z.

8.6 Read-Only Memory (ROM)

8.39. What are the contents of the ROM in Fig. P8.39? (All FETs are NMOS.)

8.40. What are the contents of the ROM in Fig. P8.40? (All FETs are NMOS.)

8.41. What are the six output data words for the ROM in Fig. P8.41?

8.42. Identify and simulate the worst-case delay path in the ROM in Fig. P8.41.

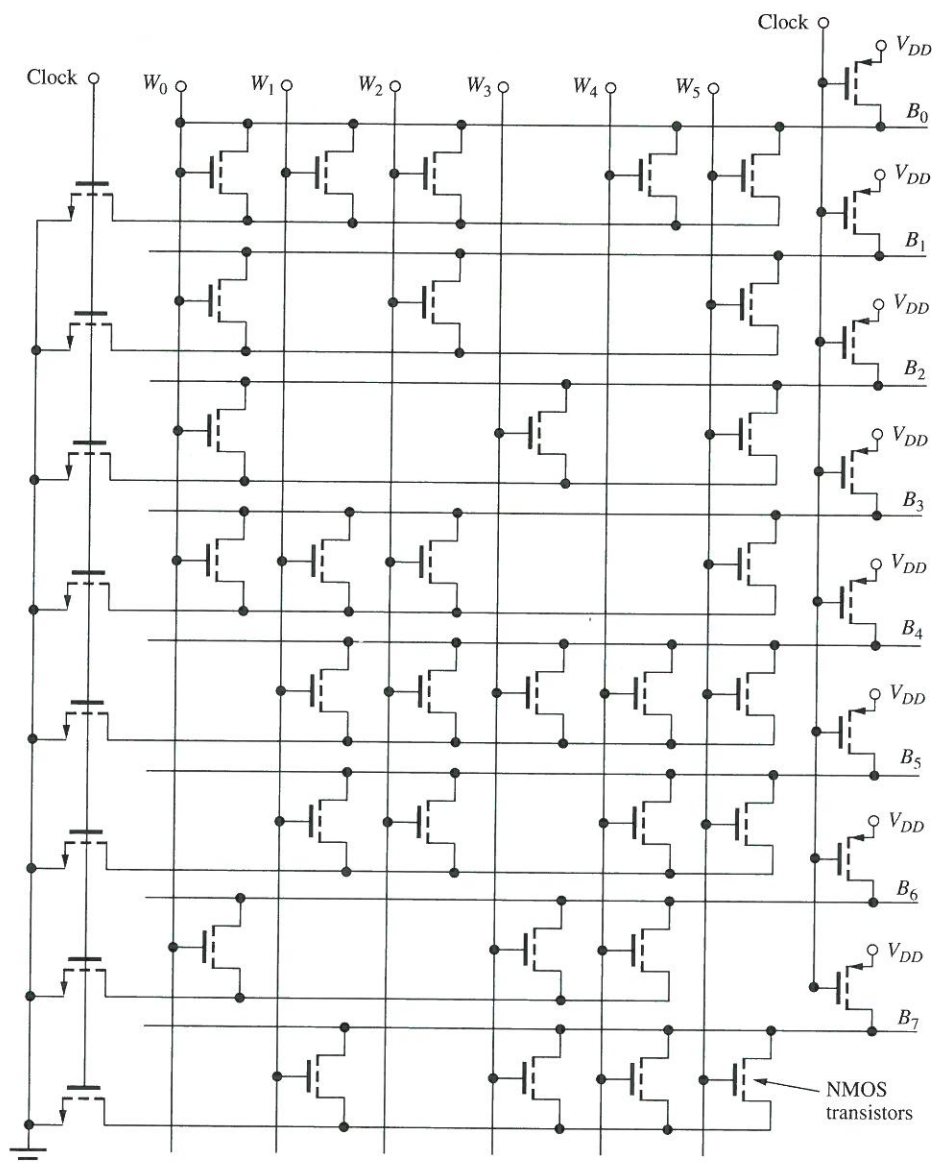8.43. Redraw the ROM circuit in Fig. 8.36 using pseudo-NMOS circuitry.

Figure P8.41

8.7 Flip-Flops

8.44. What are the logic functions of inputs 1 and 2 in the flip-flop in Fig. P8.44?

8.45. What is the minimum size of the transistors connected to the R and S inputs in Fig. P8.45 that will ensure that the latch can be forced to the desired state? Do not be concerned with speed of the latch.

8.46. Simulate the propagation delay through the D latch to Q and $\overline{Q}$ in Fig. 8.44. Assume that D is stable and the clock signal is a square wave. Assume the transistors all have $W/L = 2/1$ and use $V_{DD} = 2.5$ V. Use the transistor models on Appendix B.

8.47. Simulate the master-slave D-flip-flop with the slowly rising clock ($T = 20$ μs) in Fig. P8.47(a). Assume all $W/L = 2/1$. What happens to data on the D input? Use the transistor models in Appendix B.
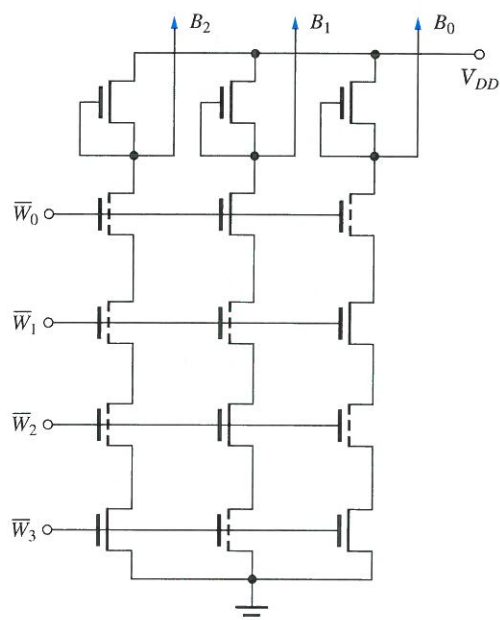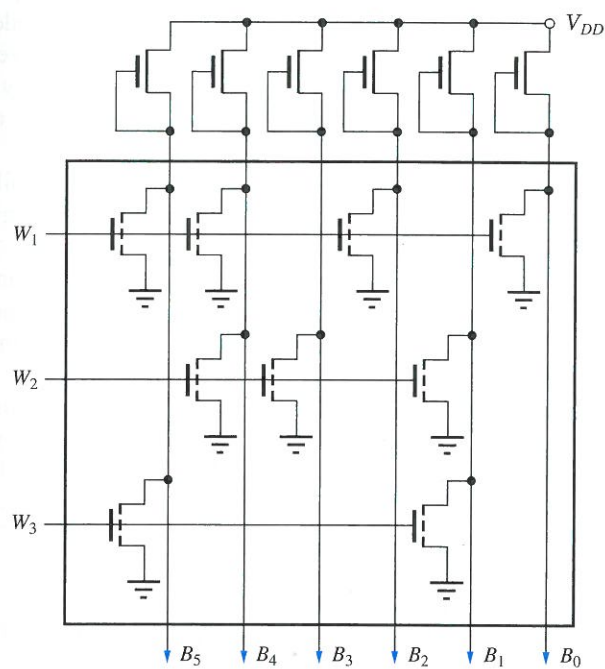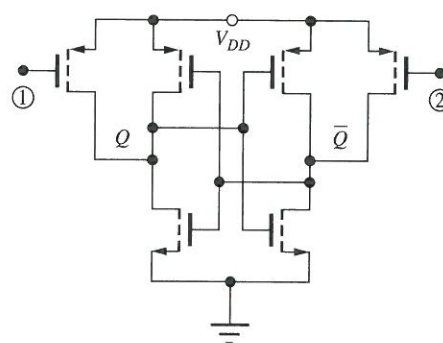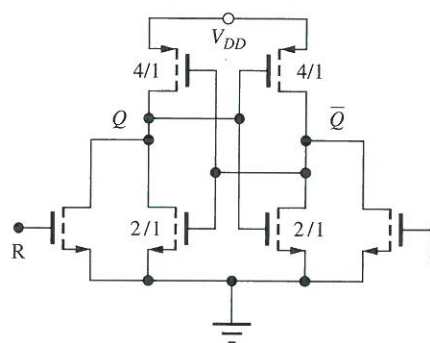
Figure P8.39

Figure P8.40

Figure P8.44

Figure P8.45

Figure P8.47