Experiment-4

FET Driver, Load, and Switch Circuits

Introduction

The objectives of this experiment are to observe the operating characteristics of inverter circuits which use JFETs and MOSFETs as driver, load, and switch devices, and to observe the effect of differing device parameters on the resulting voltage transfer characteristics (VTCs). The VTCs will be examined both using an oscilloscope and a LabVIEW curve tracer.

Precautions

Junction field-effect transistors (JFET's) involve only an internal pn-junction and are thus relatively static insensitive and may be handled freely. However, discrete MOSFETs involve a very thin gate oxide layer which may not have any static protection diodes included as part of the device. As a result, the discrete MOSFETs can be very static sensitive and must be treated properly to avoid having to buy replacements.

To avoid static discharge damage to the MOSFETs, keep their leads inserted into the black conductive foam whenever possible. Always touch a grounded object, such as the frame of the lab bench, to discharge any built-up static charges from your body before handling the MOSFET. After this, carefully remove the MOSFET from the black foam and insert it into either the curve tracer or the solderless breadboard. Pay particular attention to correctly identifying the leads on the devices. Improper connection of the device is another means in which they can be destroyed. Once the MOSFET is correctly connected into its test circuit, it is reasonably well protected from static, since there now exist resistors or power supply terminals which allow current to flow from lead to lead. As a basic rule, remember that static affects only floating terminals on a device or circuit. Simply connecting these floating terminals to ground with a large value resistor, say 1 MΩ or so, is often sufficient to provide a discharge path for any built-up charges.

This experiment will also use standard 4000-series unbuffered CMOS (metal gate) integrated circuits. These IC's have internal diodes to protect the MOSFET gates, but even so, they can still be destroyed by careless handling which may produce an electrostatic discharge (ESD) event. Follow the same precautions as for dealing with a discrete MOSFET.

To avoid static discharge damage to the IC's, keep the parts inserted into the black conductive foam whenever it is not being used in a circuit. Alternatively, the pins may be pushed into a small piece of aluminum foil, or the part may be wrapped in the foil, if some conductive black foam is not available. Always discharge any built up static charges from your body by touching a grounded metal object, such as the frame of the lab bench, before

handling the ICs. When finished with a given circuit, return the IC to the foam or the foil.

Pay attention so that none of the leads become folded underneath the IC as you press it into the breadboard. If the leads on the IC are bent excessively outward so that they do not fit well into the breadboard, you can make the leads more parallel by slightly rolling the IC on the tabletop to bend all of the leads on one side together.

Exercise the same care when removing the IC from the solderless breadboard. Often, the IC may be held quite tightly by the breadboard, making removal difficult. Use a small screwdriver blade to pry the IC up from underneath in this case. If you choose to use just your fingers to pull the IC from the breadboard, be carefull that the IC does not flip around and stick its sharp leads into your finger tip. While humans normally kill ICs with static discharges, ICs themselves can bite back in this manner! Usually, this is non-fatal.

Procedure 1 E-mode MOSFET driver with resistor load

Comment

In each of Procedures 1-5 of this experiment, you will be powering the circuits with a single +5.0 Volt DC supply and measuring the voltage transfer characteristics (VTC) using the X-Y mode of an oscilloscope. In addition, each of the circuits will be driven by a 5 V_{pp} sinewave that is produced by a function generator. Since the set-up configurations for these instruments are all the same for the first five procedures of this experiment, they will only be described once, here, in Procedure 1.

Set-Up

Turn on the power to a DC power supply and set the meter to monitor the output voltage. Plug a red squeeze-hook test lead into the positive (+) banana jack and a black squeeze-hook test lead into the negative (-) banana jack of the power supply. Adjust the output voltage to +5.0 Volts DC. The meter on the power supply will usually be accurate enough for this, but you may wish to verify this voltage with the DMM on the lab bench. If your power supply has the ability to limit the output current, set this current limit to about 10 mA, as a precaution. Leave the power supply with these settings for the duration of this laboratory experiment.

Turn on the power to a function generator, and configure it to produce a 5.0 V_{pp} (peak to peak) sinewave at a frequency of 100 Hz with a +2.5 V DC offset at its output. In other words, the output should oscillate sinusoidally between 0.0 Volts and +5.0 Volts. Turn on an oscilloscope, connect a 10× probe to both the Ch-1 and Ch-2 BNC input connectors, and verify that the function generator is producing the correct output waveform.

Next, configure the oscilloscope to display a VTC in its X-Y mode. Set the range to 1 V/div for both Ch-1 and Ch-2. This scale factor will thus apply to both the X and Y axes of the display. Set the input coupling switch on both channels to the GND position and use the Ch-2 position and horizontal position controls to center the spot exactly 1 division (1 cm) below the cross-hairs in the center of the screen. (There should be 5 divisions (5 cm) between the spot and the edge of the screen to the right, to the left, and above the spot.) Return both input coupling switches to the DC position. Leave the oscilloscope in this configuration for the duration of this laboratory experiment.

As a check of your set-up, connect the output of the function generator to both the Ch-1 (X-input) and Ch-2 (Y-input) of the oscilloscope. You should see displayed a straight line with a slope of +45 degrees extending from 1 division (1 cm) below the center of the screen up into the upper right hand corner (first quadrant), extending 5 divisions (5 cm = 5 Volts) along each axis. Do not proceed further until you obtain this display.

Comment — The above set-up is common to the first five procedures in this laboratory experiment. That which follows from here is specific only to Procedure 1.

Comment — Throughout this experiment, you will use the CD4007 CMOS integrated circuit. This is a very general purpose CMOS IC which includes 3 n-channel and 3 p-channel MOSFETs connected as shown in Fig. E4.1a. The digits by each terminal indicate the pin numbers on the 14-pin DIP package, shown in Fig. E4.1b. Note that pin 14 must *always* be connected to the positive power supply voltage, and pin 7 must *always* be connected to the most negative (or ground) power supply voltage in order to keep the body-to-source and body-to-drain pn-junctions from becoming forward biased.

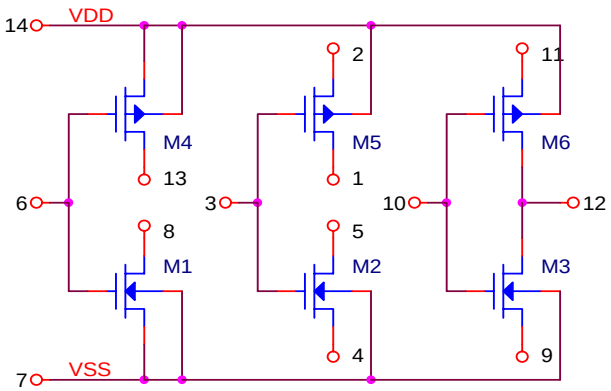

Figure E4.1a

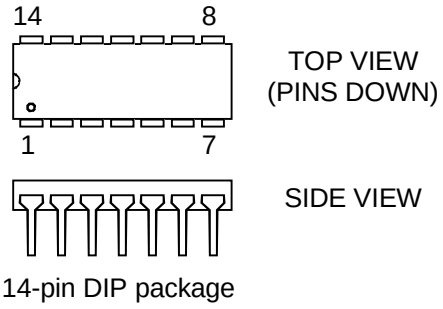

Figure E4.1b

Use a solderless breadboard to connect the circuit shown below in Fig. E4.1c using the following components:

R1 = {1.0 kΩ, 4.7 kΩ, 20 kΩ} 5% 1/4 W ***
M1 = CD4007 MOSFET array; use MOSFET M1 of the array, pins 6,7,8.
*** only one of these values will be used at a time; start with R1 = 4.7 kΩ.

Insert the CD4007 IC into a clear spot on the solderless breadboard so that the IC straddles the center groove of the breadboard. This will give each lead a separate tie point on the breadboard.

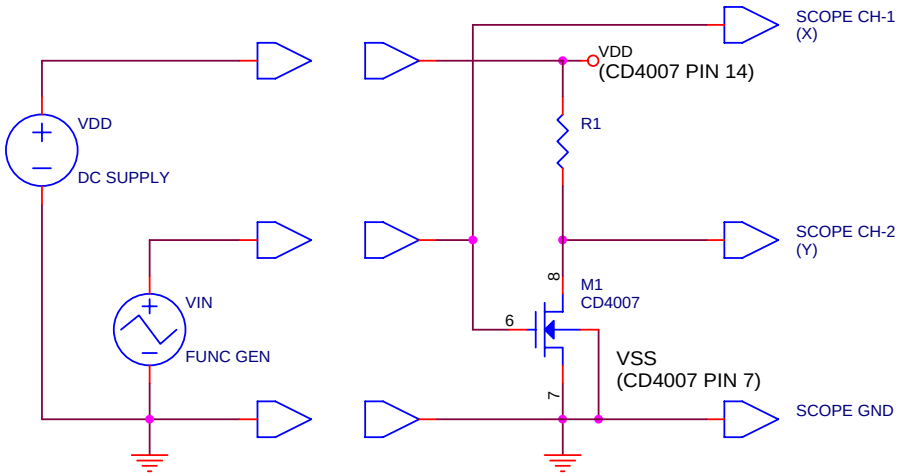

Figure E4.1c

Connect the oscilloscope ground, Ch-1 (X-input), and Ch-2 (Y-input) as shown in Fig. E4.1c. Connect the power supply ground (black lead) and positive (red lead) as shown in Fig. E4.1c. Be sure to connect the the positive VDD supply to pin 14 of CD4007 as well. Finally, connect the function generator output ground and signal leads as shown in the figure.

Measurement-1

The oscilloscope display should now show the VTC for this resistor load MOSFET driver circuit which forms a logic inverter gate. Sketch the VTC in your notebook, ticking off each axis in 1 Volt increments to match the scale factors used on the oscilloscope. Note the (v_{in}, v_{out}) coordinates for any key corner points in the characteristics.

Change the value of R1 from 4.7 kΩ to 20 kΩ and note the resulting changes in the VTC. Sketch the new VTC in your notebook, again ticking off the axes and finding the coordinates of any key corner points. You can sketch this VTC on the same set of axes as the previous one.

Change the value of R1 from 20 kΩ to 1.0 kΩ and note the changes in the VTC. Again, sketch the VTC in your notebook, tick off the axes, and find the coordinates of the key corner points. You can sketch this VTC on the same set of axes as the previous two.

Question-1

(a) In your notebook, first discuss qualitatively why the output is low when the input is high, and vice-versa, why the output is high when the input is low. Be brief, but complete in your explanation.
(b) Find the output high voltage V_{OH} and the output low voltage V_{OL} for each of the three cases measured above. Which of these parameters is dependent upon the value of R1? Explain why this is so.
(c) Which of the three values for resistor R1 produces the best VTC for a logic family? Consider the issue of noise margins and noise immunity in your answer.

Procedure 2 E-mode MOSFET driver with D-mode load device

Set-Up

Keep the set-up configurations of the power supply, the function generator, and the oscilloscope the same as they were in Procedure 1. Construct the circuit of Fig. E4.2 below on the solderless breadboard using the following components:

M1 = CD4007 MOSFET array, use MOSFET M1, pins 6, 7, & 8.
J1 = MPF102 n-channel JFET
R1 = {1.0 kΩ, 10 kΩ} 5% 1/4 W ***
*** only one of these values will be used at a time; start with R1 = 1.0 kΩ.

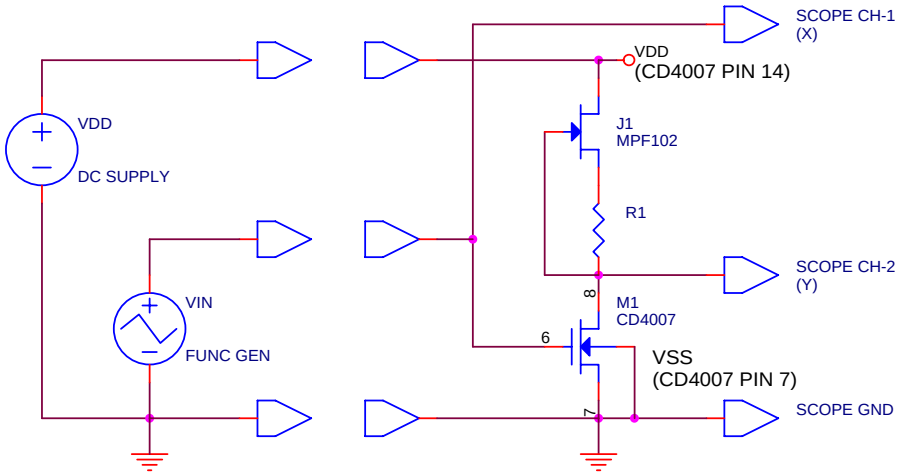

Figure E4.2

Connect the oscilloscope probes and grounds, then the power supply leads, and finally the signal generator connections as shown in Fig. E4.2.

Measurement-2

In your notebook, sketch the VTC for this inverter gate, ticking off the axes in 1 Volt divisions and finding the coordinates for the key corner points in the characteristic.

Change the value of R1 from 1.0 kΩ to 10 kΩ. Sketch the new VTC on the same set of axes as the previous one. Indicate which curve is associated with each value of resistor R1.

Question-2

(a) Qualitatively discuss the differences in the VTC between a resistor load and a depletion-mode load device.
(b) Which gives the better performance as a logic inverter gate? Explain your answer.
(c) Does the resistor load or the depletion-mode load produce a higher gain?
(d) Qualitatively explain why increasing R1 to 10 kΩ produces a better VTC.

Procedure 3 D-mode JFET driver with resistor load

Set-Up

Keep the set-up configurations of the power supply and the oscilloscope the same as they were in Procedure 2. Construct the circuit of Fig. E4.3 below on the solderless breadboard using the following components:

J1 = MPF102 n-channel JFET
R1 = {470 Ω, 1.0 kΩ, 10 kΩ} 5% 1/4 W ***
R2 = 1.0 kΩ 5% 1/4 W
*** only one of these values will be used at a time; start with R1 = 1.0 kΩ.

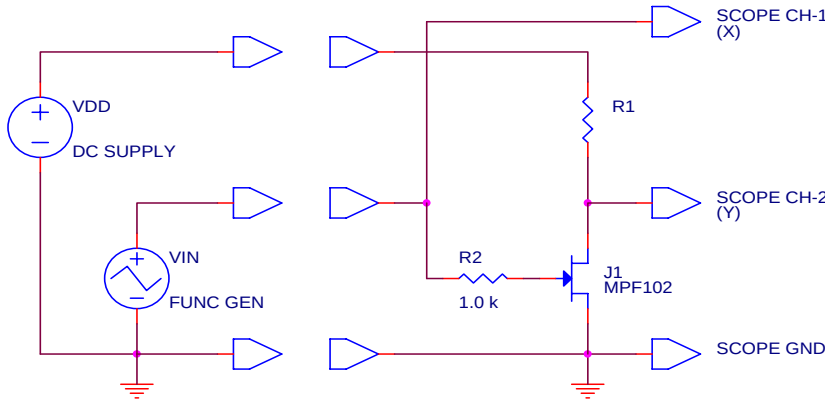

Figure E4.3

Reconfigure the function generator to now output a 10 V_{pp} (peak-to-peak) sinewave at 100 Hz with zero DC offset. That is, the output should be a sinewave of 5 V peak amplitude, centered about a DC level of zero.

Connect the oscilloscope probes and grounds, then the power supply leads, and finally the signal generator connections as shown in Fig. E4.3. You may need to change the range settings for Ch-1 and Ch-2 to 2 V/div in order to fit the larger VTC within the oscilloscope display.

Measurement-3

In your notebook, sketch the VTC for this inverter gate, ticking off the axes in 1 Volt divisions and finding the coordinates for the key corner points in the characteristic. Note that you will have to include both quadrants 1 and 2 of v_{out} versus v_{in}.

Change the value of R1 from 1.0 kΩ to 10 kΩ and sketch the new VTC on the same set of axes as the previous one. Change the value of R1 from 10 kΩ to 470 Ω and sketch the new VTC on the same set of axes as the previous one. Label each VTC to indicate which value of R1 produced it.

Question-3

(a) In your notebook, briefly describe the principal difference in the VTC between an E-mode driver versus a D-mode driver when used to form a logic inverter gate.
(b) Explain why the D-mode driver would require an additional power supply voltage to form a logic family.

Procedure 4 CMOS inverter circuit

Set-Up

Keep the set-up configurations for the DC power supply and the oscilloscope the same as they were in Procedure 3. Remove all of the parts from the solderless breadboard. Reconfigure the function generator to again output a 5 V_{pp} (peak-to-peak) sinewave at a frequency of 100 Hz with a DC offset of +2.5 Volts. That is, the positive peak of the sinewave should be at +5.0 Volts and the negative peak of the sinewave should be at 0.0 Volts.

Connect the circuit shown below in Fig. E4.4 using MOSFETs M1 and M4 on the CD4007 array.

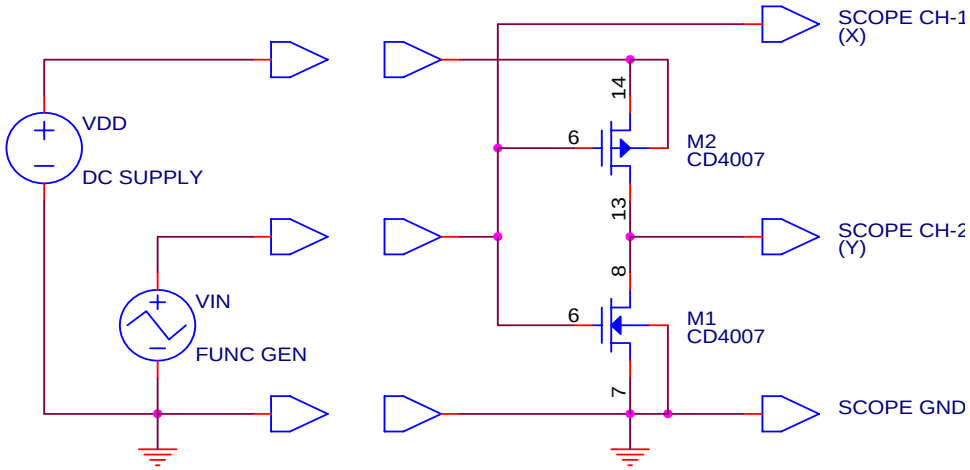

Figure E4.4

Connect the oscilloscope probes and grounds, then the power supply leads, and then the function generator leads to the breadboard as shown in Fig. E4.4.

Measurement-4

Sketch the resulting VTC in your notebook, ticking off the axes in 1 Volt divisions, and finding the coordinates for all key corner points on the characteristics.

Question-4

(a) In your notebook, comment on the symmetry (or lack of symmetry) in the observed VTC.
(b) Comment on if the CMOS VTC is any better or worse than the VTC for the resistor load E-mode driver inverter circuit in terms of noise margins and signal swings.
(c) From your measured VTC of the CMOS inverter circuit, estimate the threshold voltage of both the n-channel and the p-channel MOSFETs.

Procedure 5 CMOS Schmitt trigger circuit

Set-Up

Keep the power supply, the oscilloscope, and function generator in the same set-up configuration as was used in Procedure 4. Also keep the CD4007 IC plugged into the solderless breadboard. Simply disconnect the power supply, function generator, and oscilloscope probes from the breadboard, remove any jumper wires, and reconnect the CD4007 IC to produce the circuit shown below in Fig. E4.5a. Be sure to check your connections very carefully, as it is very common and easy to miscount the pin numbers on the IC.

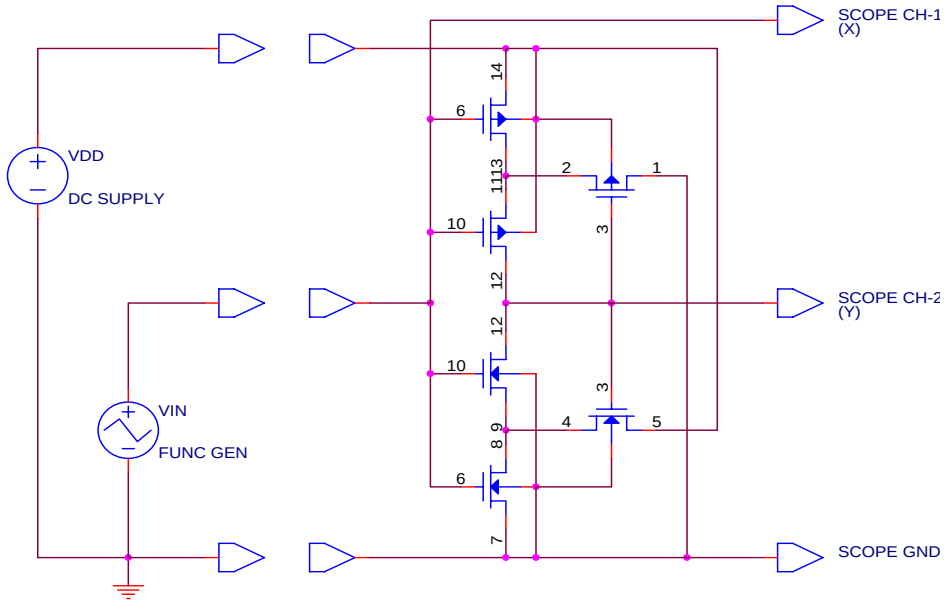

Figure E4.5a

Connect the oscilloscope probes and grounds, the power supply leads, and then the signal generator leads to the breadboard as shown in Fig. E4.5a.

Measurement-5

Sketch the resulting VTC in your notebook, ticking off the axes in 1 Volt divisions, and finding the coordinates for any key corner points. Because of the bistable nature of this circuit, the vertical parts of the VTC may appear very faint on the oscilloscope, if they are even visible at all. In your sketch, try to fill in the missing parts that the oscilloscope does not show. These characteristics should show a strong degree of hysteresis, meaning that the vertical transition upward occurs at a different input voltage from the vertical transition downward.

Now disconnect the signal generator and the oscilloscope probes from the breadboard. Connect a red T-1 LED (LED1) and a 2N7000 MOSFET (M1) between the output of the Schmitt trigger circuit and the power supply rails, as shown in Fig. E4.5b below. Pay attention to correctly installing both the MOSFET and the LED. Remember that the anode or (+) lead of the LED is the longer of the two. Next, connect a 10 kΩ potentiometer (R1) between the

power supply and ground connections and connect the wiper of the potentiometer R1 to the input to the Schmitt trigger circuit, as shown in Fig. E4.5b.

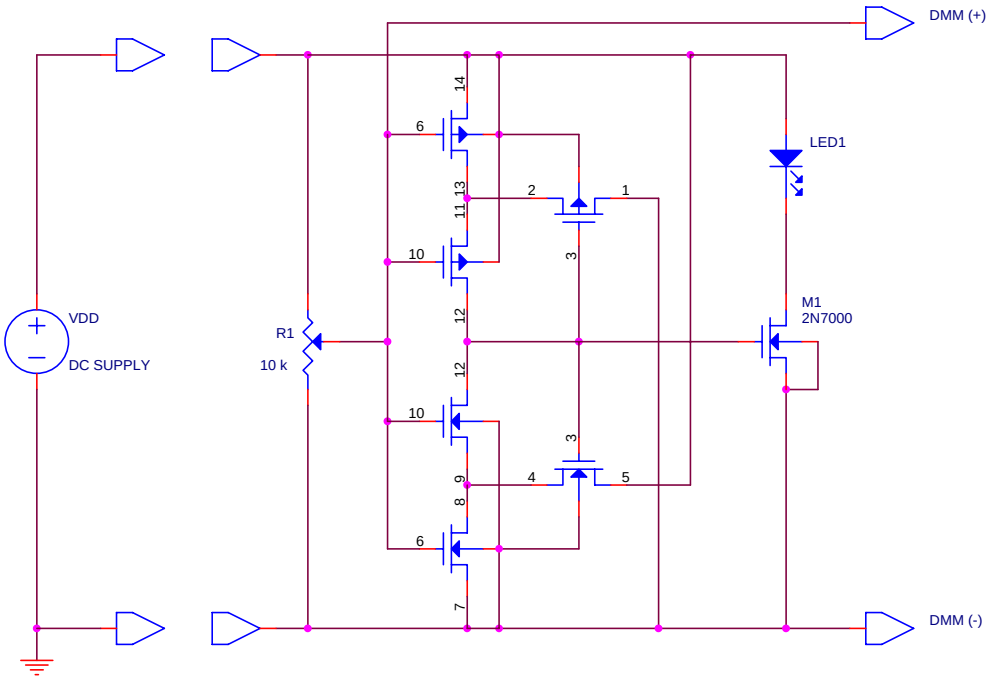

Figure E4.5b

Initially adjust R1 to put VDD = +5.0 V at the input to the Schmitt trigger circuit. At this point, LED1 should be off. Slowly turn R1 to lower the voltage input to the Schmitt trigger and stop just at the point where LED1 turns on. Measure the input voltage at this point with the bench DMM. Now slowly turn R1 in the other direction to increase the voltage input to the Schmitt trigger circuit and stop just at the point where LED1 turns off. Measure the input voltage at this point with the bench DMM.

Question-5

(a) Explain qualitatively what is unusual about these voltage transfer characteristics, as compared to the preceding ones.
(b) The hysteresis voltage is the separation in the two curves as measured along the v_{in} axis. Determine the hysteresis voltage for this circuit from your VTC measurements on the oscilloscope. Compare this value of hysteresis voltage with the difference between the two DMM readings which mark the transition voltages for the LED. Use this information to put arrows on your VTC which indicate the direction that the circuit voltages follow for the upward and downward transitions.
(c) Describe how this circuit would be useful for rejecting noise on a digital input signal.

Procedure 6 Create a VTC curve tracer using LabVIEW and a DAQ card

Comment

The objective of this procedure will be to construct a LabVIEW curve tracer that can be used to examine and record the VTCs of various FET circuits. Most of the VTCCurveTracer.vi has already been written, but in this procedure the core data acquisition routine will be constructed as a sub-VI to gain some familiarity and practice in setting up and using the analog inputs and analog outputs of a data acquisition (DAQ) card.

Set-Up

Into a directory on one of the lab computers, copy in the files: VTCCurveTracer.vi, VTCStepGenerator.vi, VrefArray.vi, and ShowPrevious.vi. Launch LabVIEW 7.1 on the computer and open up the file VTCCurveTracer.vi. The front panel of the VI should appear as shown in Fig. E4.6a below.

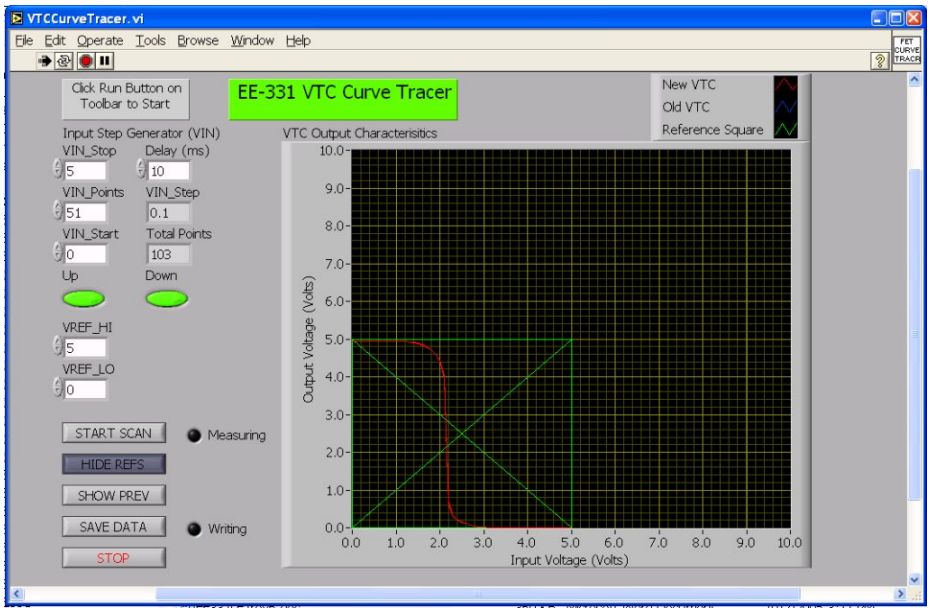

Figure E4.6a

The VTC curve tracer functions by scanning the input voltage VIN from a VIN_Start value to a VIN_Stop value using VIN_Points. If the Up button is selected, the scan goes from VIN_Start to VIN_Stop, and if the Down button is selected, the scan goes from VIN_Stop to VIN_Start. If both buttons are selected, the scan first goes up and then back down. At each value of VIN, the output voltage VOUT of the test circuit is measured. After the scan is complete, a plot of VOUT versus VIN is displayed on the graph. The basic operation is very similar to the Diode and FET curve tracers that were used in previous experiments.

This curve tracer has a few additional features, one of which is the ability to display a reference square along with the measured data on the graph. The reference square is constructed between values of VREF_HI and VREF_LO

which are input from the front panels controls. Pressing the SHOW REFS button will add the reference square to the graph without disturbing the data. Likewise, pressing the button again (now labeled as HIDE REFS) will remove the reference square.

The VTC curve tracer also has the ability to measure and compare two different VTCs. By pressing the SHOW PREV button, the previous VTC that was measured will be added to the graph without disturbing the results of the current measurement. Obviously, the START SCAN button must have been pressed at least twice before this will do anything. Pressing the button again (now labeled as HIDE PREV) will remove the previous VTC from the graph.

The SAVE DATA button works similarly to that on the other curve tracers; pressing the button will bring up a dialog box that will allow the user to specify a location and filename for an Excel spreadsheet file that contains the measured data. The SAVE DATA command will create an Excel spreadsheet with 6 columns of data: VIN and VOUT for the new VTC; VIN and VOUT for the previous VTC (for comparison purposes), and eight (VIN, VOUT) ordered pairs which will create the reference square.

Next, press Ctrl+E to open the VTC curve tracer block diagram, shown in Fig. E4.6b below. In your case, the sub-VI labeled "VTC MEAS" in the center of the For-loop will not be present; you will add it later on as part of this procedure.

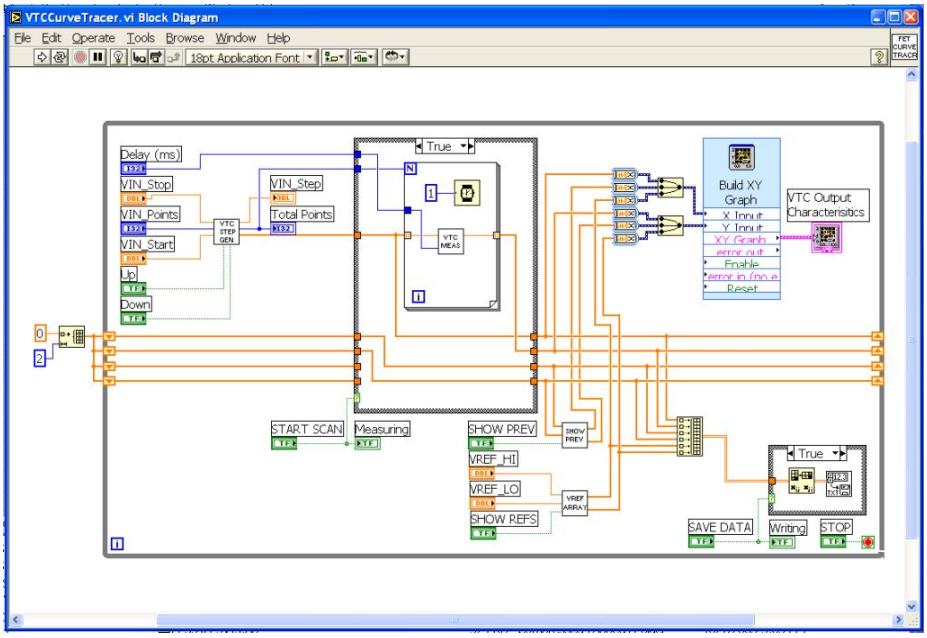

Figure E4.6b

The structure of the VTC curve tracer starts with an overall While-loop which runs until the STOP button is pressed. Within this While-loop, local variables are created as shift registers for the present and the previous X and Y data

arrays. These appear as the four long horizontal orange wires in the block diagram. Each of these are initialized to a simple "null" plot which simply puts a point at the origin. The output graph is set up to display three plots of (X,Y) data. The first set is the present VTC data, the middle set is the previous VTC data, and the last set is the data points which create the reference square. All six of these 1-D arrays are combined into a single 2-D array which is passed to the true/false case statement which writes the data out to a spreadsheet file (located in the lower right corner of the block diagram). The ShowPrevious.vi sub-VI selects either the previous data or a null plot to display on the graph. The VRefArray.vi sub-VI selects either the 8 (X,Y) pairs that will create the reference square or a null plot. This is how the previous VTC and the reference square are turned on and off on the graph.

The VTCStepGenerator.vi sub-VI creates a 1-D array of VIN test points and passes this array to the true/false case structure which controls the measurement scan. Also passed to the measurement scan are the number of points and the delay in milliseconds that is to be used between each measurement. The true/false case structure shifts the last VTC data to the previous VTC data arrays and loads the present VTC data arrays with the new VIN and VOUT scanned data.

The missing sub-VI will be named VTCMeasurement.vi and its function will be to take each value of VIN, send a command to the DAQ card to output this voltage on one of the analog output channels (AO-0), wait for Delay milliseconds, and then read one of the DAQ card analog input channels (AI-7), and return this value as VOUT.

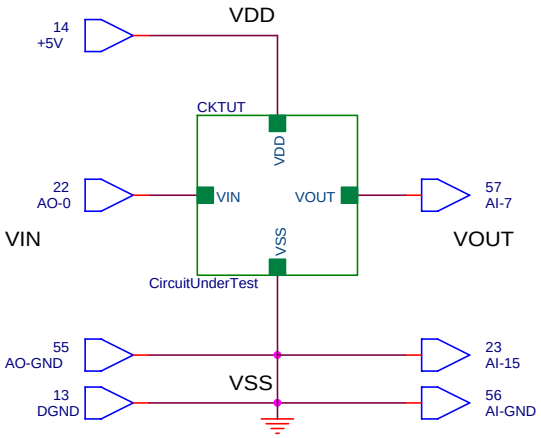

Figure E4.6c

Figure E4.6c shows how the DAQ card will be connected to the circuit-under-test (CKTUT). The analog output channel-0 will be taken from the DAQ card from pin #22 (AO-0) to pin #55 (AO-GND), and the analog input channel-7 will be taken from the DAQ card as a differential input between pin #57 (AI-7) and pin #23 (AI-15). The analog input ground, pin #56 (AI-GND) will be tied to the analog output ground, pin #55 (AO-GND), and the (–) input of

VOUT, pin #23 (AI-15). To power up the circuit-under-test, if needed, a +5V digital power supply can be obtained from the DAQ card from pin #14 (+5V) and pin #13 (DGND).

Create a VI

From the LabVIEW 7.1 File menu, select NEW VI, and both a new front panel and block diagram window will open. In the front panel window, first place two numeric controls, VIN and Delay, and one numeric indicator, VOUT, as shown in Fig. E4.6d below.

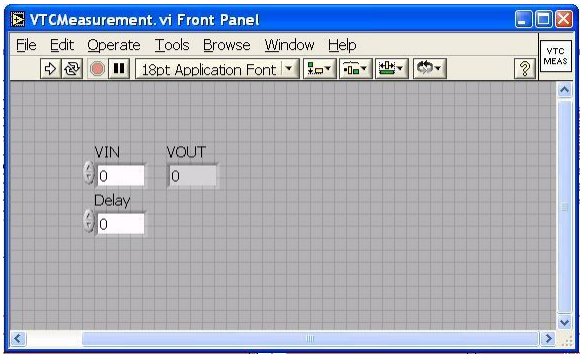

Figure E4.6d

Switch to the block diagram window. Icons for VIN, VOUT, and Delay should already appear there. Add a stacked sequence structure, which appears like a roll of film. Right click on the frame counter at the top, and add frames until you get a total of 3, which are named {0,1,2}. Add a DAQ Assistant to frame-0, and set up the DAQ assistant for an analog output of volts, over a range of –10 V to +10 V, and using analog output channel AO-0. Then wire the VIN numeric control through the stacked sequence structure to connect to the data input of the DAQ assistant, as shown in Fig. E4.6e below.

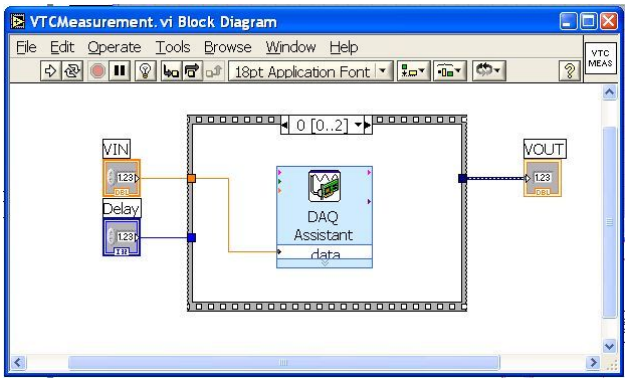

Figure E4.6e

Next, switch to frame-1 and add a Wait (ms) block, which looks like a wristwatch. Wire the Delay numeric control through the stacked sequence structure and connect it to the input of the Wait (ms) block.

Next, switch to frame-2 and add another DAQ Assistant. Set this one up for an analog input of volts, over a range of –10 V to +10 V, differential mode,

and using analog input channel AI-7. Finally, wire the VOUT numeric indicator back through the stacked sequence structure to connect to the data output of the DAQ Assistant.

At this point, save your work as VTCMeasurement.vi, using File > Save, or Ctrl+S, making sure the directory is the same as where the other VTC curve tracer VIs are located.

At this point, you may wish to pretty-up the icon that will be used to represent the VI. Do this by right clicking on the VI icon in the front panel window and select Edit Icon … Use the writing tools to fix up the icon any way that you like. For the example above, the icon was simply changed to say "VTC MEAS" using the alpha tool.

Next, right click on the VI icon in the front panel window again, and select Show Connector. This changes the icon into a pattern which shows how the various inputs and outputs will be placed when the VI is used as a sub-VI. Delete all of the existing connections, and then select a pattern which is a 2x2 array. Using the wiring tool, first click on the upper left square of the pattern, and then click on the VIN numeric control of the front panel. Finally, click anywhere else on the front panel and the upper left square of the pattern should turn orange, corresponding to the real number format of the VIN control. Use this same procedure to wire the VOUT indicator to the upper right square, and the Delay control to the lower left square of the pattern. When you are finished, just right click on the icon once more and select Show Icon. Save the file again to make these changes permanent.

The last step is to add this sub-VI to the VTCCurveTracer.vi. Go to the VTCCurveTracer.vi block diagram and add the VTCMeasurement.vi that you just created using the Select VI … button of the functions pallet. Select the VTCMeasurement.vi and then move the cursor to the center of the For-loop and drop the sub-VI there. Use the wiring tool to connect the VIN, Delay, and VOUT connections of the sub-VI to the For-loop, as shown in Fig. E4.6b. Finally, save the VTCCurveTracer.vi, and you are done with the software part!

DAQ Wiring

The output of the DAQ card must be wired up according to the schematic of Fig. E4.6c. Using either the CB-68LP or CB-68LPR connector blocks, make the same connections with some long (approx. 6-8 inch) lengths of hook-up wire, so that the connections can be brought over to a solderless breadboard for testing a circuit there. Figure E4.6f shows the connections on the CB-68LP connector block: yellow = VOUT(+) (AI-7), brown = VOUT(–) (AI-15), blue = VIN(+) (AO-0), white = VIN(–) (AO-GND), and the short red wire connects AO-GND to AI-GND. Also shown on the right side of the connector block are the +5V digital power supply outputs: red = +5V and black = DGND.

Figure E4.6f

Measurement-6 Perform a quick self-test of the VTC curve tracer as follows. Connect the VIN DAQ output to the VOUT DAQ input (yellow to blue), and connect the analog output ground to the analog input ground (brown to white). This should make VOUT = VIN.

Start the VTCCurveTracer.vi by clicking the Start button on the toolbar. Enter a scan from 0.0 V to +5.0 V with 11 points, going up and down, (0.5 V/step, 23 total points), and enter VREF_HI = +5.0 V, and VREF_LO = 0.0 V. Enter a Delay of 10 ms. Click on the SHOW REFS button and a green reference square from 0.0 to +5.0 Volts should appear on the graph. Click on the START SCAN button and the measurements should procede, finally adding a red straight line to the graph that lies directly on top of the VIN = VOUT diagonal of the reference square. If this works, then you are in business! Click on the STOP button and make sure that your new VIs are all saved.

Question-6 (a) Based upon the structure of VTCCurveTracer.vi, if Delay = 10 ms and Total Points = 103, how long would the complete scan take to perform?
(b) Suggest a method by which a CLEAR DISPLAY button could be added to the VTCCurveTracer.vi to clear the graph after a measurement has been made. You do not need to create the actual VI for this; just describe how you would go about it.

Procedure 7 CMOS inverter VTC measured using a LabVIEW curve tracer

Comment

In this procedure, the LabVIEW VTC curve tracer that was created in Procedure 6 will be used to measure and record the VTC of a CMOS inverter, essentially the same circuit that was examined in Procedure 4. The LabVIEW VTC curve tracer can be used to examine any of the circuits of Procedures 1-5, with the only limitation being that the DAQ card only provides a power supply voltage of +5 Volts for use as VDD and VSS. If a different power supply voltage is required, this must be supplied to the circuit-under-test by an external DC power supply. If an external DC power supply is used for this, be VERY careful with the connections so that the DC power supply does not connect to the DAQ card outputs and burn them out!

Set-Up

If it is not running already, launch LabVIEW 7.1 and open the VTCCurveTracer.vi. If it has not already been done, wire up the connector block as described in Procedure 6 to provide long jumper wires for connecting VIN, VOUT, VDD, and VSS to a solderless breadboard.

On a solderless breadboard, wire up the CMOS inverter shown in Fig. E4.7a below using MOSFETs M3 and M6 of a CD4007 CMOS MOSFET array. This is essentially the same CMOS inverter that was used in Procedure 4, but made from MOSFETs M3 and M6 instead of MOSFETs M1 and M4. Any of the three possible CMOS inverters that can be made from a CD4007 will work identically for this procedure.

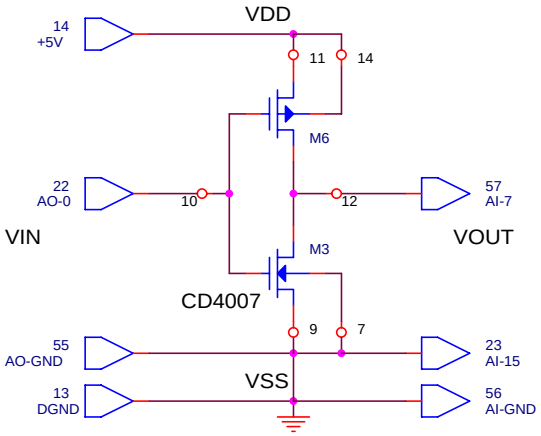

Figure E4.7a

The wiring on the solderless breadboard is shown in Fig. E4.7b below, using the same color-coded wires as in Fig. E4.6f. This is only one of many possible ways to make the connections. Pay close attention to the VDD and VSS power supply wires so that you do not accidentally short out the +5V DC power supply on the DAQ card!

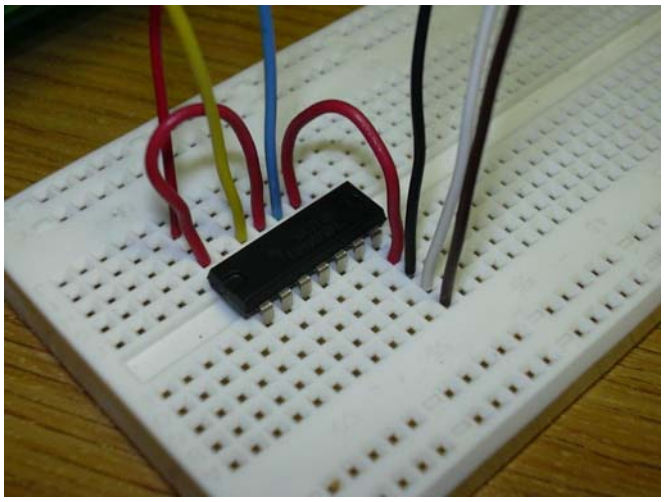

Figure E4.7b

Measurement-7 Start the VTCCurveTracer.vi by clicking the Start button on the toolbar. Enter a scan from 0.0 V to +5.0 V with 21 points, going up and down, (0.25 V/step, 43 total points), and enter VREF_HI = +5.0 V, and VREF_LO = 0.0 V. Enter a Delay of 10 ms. Click on the START SCAN button and after the measurement sequence is complete, the graph should show a red VTC for the CMOS inverter which closely resembles that measured in Procedure 4.

Click on the SHOW REFS button to add a green reference square to the graph. The difference between the measured VTC and the VIN = ±VOUT diagonals highlights how well the CMOS inverter is performing as a regenerative logic gate.

Click the START SCAN button again to take another VTC scan, and then click the SHOW PREV button to see if there is any difference between the two. This is always a good thing to do, to insure that your measured data is reproducible.

Finally, click the SAVE DATA button to bring up a dialog for saving the data to an Excel spreadsheet. Click on the STOP button to halt the VI, and examine the contents of the spreadsheet file to insure that you have recorded the data correctly.

Question-7 (a) From your spreadsheet data, compute gain of the CMOS inverter at the middle of its characteristic, where the VTC is most vertical. The gain is the derivative of the VTC, dVOUT/dVIN.
(b) Give a qualitative explanation for why the VTC might not be perfectly symmetrical.
(c) At what value of input voltage VIN does the maximum current flow through the CMOS inverter?

Procedure 8 3-input CMOS NAND gate

Set-Up

Configure the DC power supply to output +5.0 Volts. Insert the CD4007 CMOS MOSFET array into a clear area of the solderless breadboard (if it is not already there), and wire up the circuit shown below in Fig. E4.8.

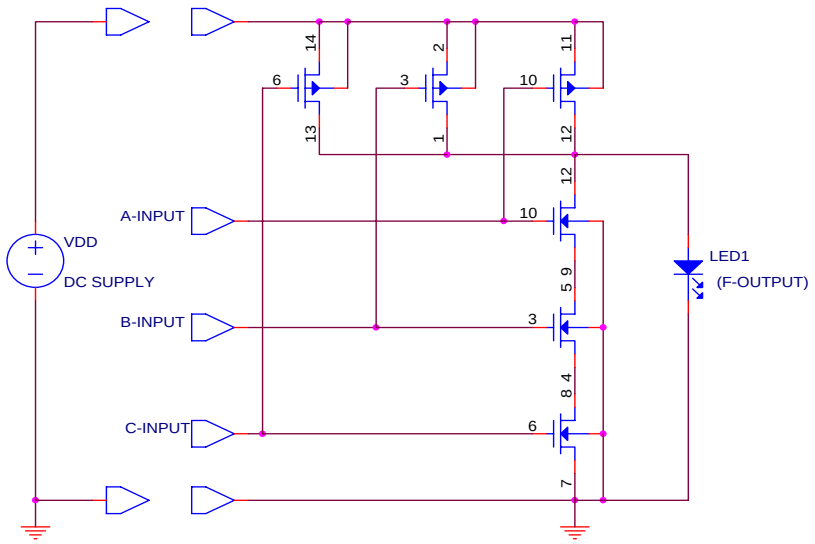

Figure E4.8

Connect the red T-1 LED between the output of the circuit and the negative (ground) power supply connection. Make certain that it is installed in the correct polarity. Connect one end of each of three 2 inch long jumper wires to each of the inputs to the circuit (A, B, and C) and then connect the positive and ground leads of the DC power supply to the circuit.

Measurement-8

In your notebook, make a truth table for this logic gate circuit, giving the output state for each possible input combination of A, B, and C. Note that the output is a logical "1" or HIGH level when the LED is ON. Simply connect the three 2 inch long jumper wires on the inputs to either the positive or ground power supply connections to produce an input "1" or "0" signal.

Question-8

(a) Verify in your notebook that the circuit of Fig. E4.8 does indeed form a 3-input NAND gate in CMOS.
(b) In your notebook, design a circuit to implement a 3-input NOR gate in CMOS using a single CD4007 IC. Be sure to label the pin numbers on the IC to show how it must be connected. Remember that pin 14 must be connected to the positive power supply rail, and pin 7 must be connected to the ground rail. If you have time, you may wish to wire this circuit up and check its truth table for proper operation.

Procedure 9 CMOS analog switch characteristics

Set-Up

Keep the DC power supply set to +5.0 Volts output, and clear all parts from the solderless breadboard. Insert a CD4016B IC into the breadboard so that it straddles the center groove. Connect the power supply ground lead to pin 7 and then connect the +5.0 Volt power supply lead to pin 14.

Comment

A CMOS *transmission gate* is a subcircuit which is composed of an n-channel and a p-channel MOSFET with their corresponding drains and sources connected together. It is a four-terminal subcircuit, when the power and ground connections to the MOSFET bodies are ignored. A CMOS *analog switch* consists of a transmission gate and two more transistors to form an inverter which is used to apply opposite binary logic levels to the two gates of the transmission gate. Ignoring the power and ground connections, the analog switch is a three-terminal subcircuit. The complete circuit for an analog switch is shown as the left-most circuit in Fig. E4.9a. Since this subcircuit occurs so frequently in CMOS circuitry, several standard shorthand symbols have evolved to denote it. The middle circuit of Fig. E4.9a uses a standard logic symbol to represent the CMOS inverter and also uses the standard symbol for a CMOS transmission gate, which is essentially an n-channel and p-channel MOSFET placed back to back. The substrate connections are left implicit in this symbol. The rightmost circuit in Fig. E4.9a is one of the many symbols used to represent the complete CMOS analog switch.

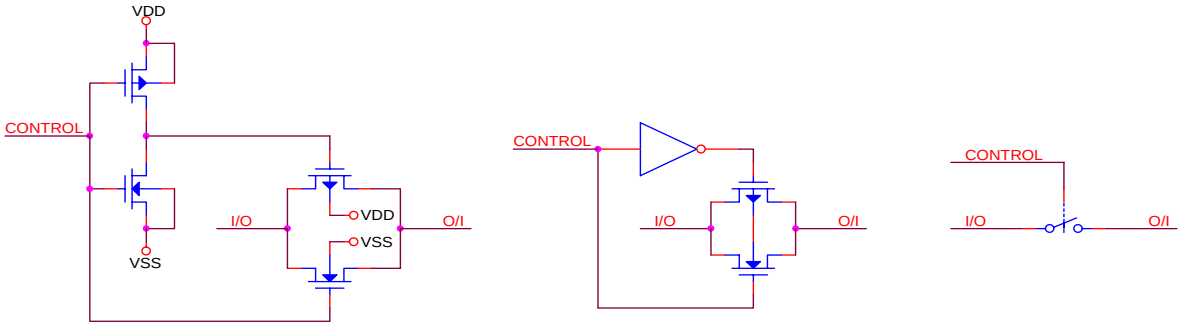

Figure E4.9a

The CD4016B integrated circuit is a quad bilateral analog switch, meaning that it contains four complete analog switch subcircuits, all fabricated on the same slab of silicon and housed in the same 14-pin DIP package. A pin-out diagram for the CD4016B is shown in Fig. E4.9b, and you should refer to this pin-out for properly connecting the IC in the following procedures. Note that the positive power supply lead must *always* be connected to pin 14, and the ground or negative power supply lead must *always* be connected to pin 7, as was the case for the CD4007 IC.

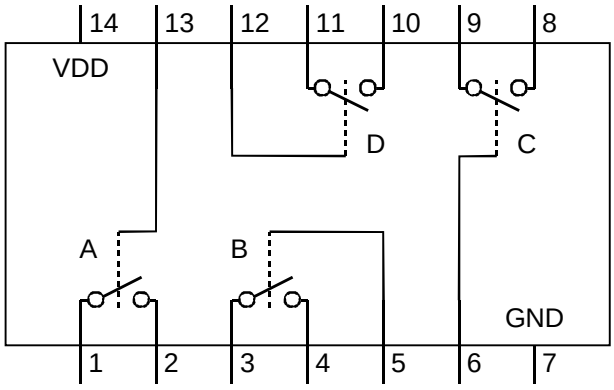

Figure E4.9b CD4016B Quad Bilateral Analog Switch

This represents a very common packaging strategy for small-scale integration (SSI) level circuits, i.e. using one package and power/ground connections to house several of the same type of subcircuit. When large numbers of the subcircuits are needed, this reduces the amount of power and ground interconnections that are needed, as well as reducing the total number of DIP packages that must be soldered on to a circuit board. However, if only one or two of the subcircuits are needed, then one is forced to buy all four of the subcircuits (in this case), whether they are needed or not.

Measurement-9 Connect and configure a bench DMM to measure resistance between the two I/O pins of the first analog switch in the package, i.e. between pins 1 and 2. The analog switch only provides a low resistance between the two I/O pins as long as the voltages on both of the I/O pins fall within the 0.0 to +5.0 V power supply window. Because the bench DMM test voltage is floating with respect to the analog switch, it is necessary to add an additional wire to insure that both of the DMM leads fall within this range. This can be done by either connecting the red (positive) DMM lead to pin 14 (VDD), *or* by connecting the black (negative) DMM lead to pin 7 (GND). Use a short length of #22 AWG solid wire to accomplish this.

Connect the control pin 13 to ground and record the "OFF" resistance of the switch in your laboratory notebook. This is normally a very high value and may exceed the range of the bench DMM. If this is the case, just list the value as "greater than 20 MΩ," which is the usual resistance range limit for most DMMs.

Now disconnect the control pin 13 from ground, and reconnect it to the positive +5.0 V power supply voltage buy just connecting pins 13 and 14 together. Record the "ON" resistance of the switch in your laboratory notebook. Switch the reference potential for the DMM to the opposite side of the 0.0 to +5.0 V window, and record the "ON" resistance for this case. One feature of an analog switch is that its "ON" resistance varies somewhat with

the level of the signal voltage on the I/O terminals. You should observe a slight difference between these two ends of the window.

Using what you have learned from the previous procedures, configure the function generator and an oscilloscope to display the voltage transfer characteristics of this analog switch in the "ON" state. Consider pin 1 as the input, and pin 2 as the output. Attach a 1 kΩ resistor between pin 2 and ground to act as a load. No other specific instructions will be given here; you are on your own for this one. If you blow out the switch in your first attempt, the package provides you with three more opportunities to get it right. Record the resulting VTC in your laboratory notebook, ticking off each axis in 1 Volt increments.

Question-9

(a) If the control voltage to the switch is at ground, what is the region of operation that the n-channel and p-channel MOSFETs of the transmission gate are in?
(b) If the control voltage to the switch is at VDD, determine the region of operation of both MOSFET's of the transmission gate if both I/O terminals are at VDD.
(c) If the control voltage to the switch is at VDD, determine the region of operation of both MOSFET's of the transmission gate if both I/O terminals are at ground.

Procedure 10 CMOS analog switch logic circuits

Comment

The CMOS transmission gate is a non-traditional building block for logic circuits. As such it introduces some unique possibilities for constructing various logic functions that are extremely compact. Because of the ease in which a CMOS transmission gate or analog switch can be constructed, CMOS logic circuits often look quite a bit different from the same arrangement of gates using only NAND and NOR functions. Sometimes these are referred to specifically as "transmission gate logic," or "analog switch logic."

One of the most fundamental features of the CMOS transmission gate is that when the gate is in its OFF state, the output node of the gate is essentially floating, being connected to neither power supply rail by a conducting MOSFET. Under such circumstances, the output node of the transmission gate would be in a "high-impedance" or "HiZ" state. The high impedance state of an OFF transmission gate is an essential element of logic circuits which must interface to bidirectional busses, such as the data buss of a microcomputer. The high impedance state of the gate disables the gate from transmitting a signal onto the buss, and instead allows another gate to do the transmitting without buss contention. Such bidirectional logic lines are also very common in serial data ports, data multiplexers, and within memory circuits.

Set-Up

Construct the circuit of Fig. E4.10a below using the CD4016B IC (denoted as U1 in the schematic) which should still be plugged into the solderless breadboard. Configure the bench DMM to measure the output voltage from the output marked F. Connect four short lengths of #22 AWG solid wire to the A, B, C, and D inputs; these will be connected to either VDD = +5.0 Volts, or ground to produce logic 1 or 0 inputs to the circuit.

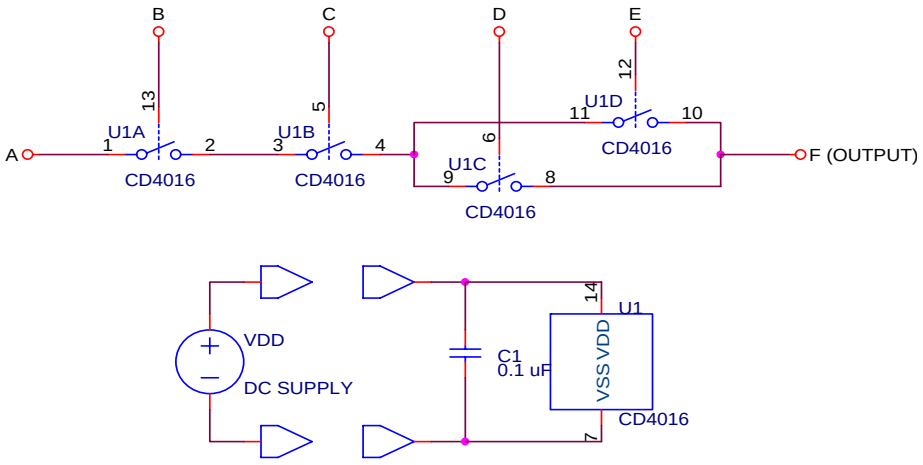

Figure E4.10a

Measurement-10

By successively connecting the A, B, C, and D inputs to VDD or ground, experimentally determine the truth table for this circuit. Your truth table

should contain all 16 possibilities of the inputs. For each of the possible output levels at F, determine whether the output is a logic “0”, a logic “1”, or a high impedance state, “HiZ.” The bench DMM will directly give the output voltage for a logic “1” or logic “0”, but you will have to use the DMM to measure resistance to one or the other of the power supply rails to determine if the output node is in the “HiZ” state.

As a final exercise, construct the circuit shown in Fig. E4.10b below, using the CD4016B to implement the two analog switches and an additional CD4007 to implement the two CMOS inverter gates. It is up to you to devise the correct circuit connections. Be sure to add a 0.1 μF power supply decoupling capacitor across each of the two IC's. Measure and record the truth table for this circuit, listing an output state of {0, 1, HiZ} for the output F.

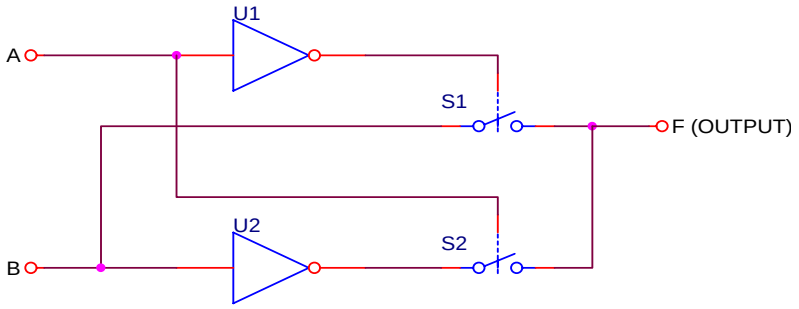

Figure E4.10b

Question-10

(a) Draw a complete circuit schematic, detailing each MOSFET explicitly, that produces a 2-input data multiplexer. Look carefully at the structure of the circuit of Fig. E4.10b for a hint on how to do this.
(b) The circuit of Fig. E4.10b implements an exclusive OR (XOR) function using a total of 12 MOSFET's. Draw a complete circuit schematic, detailing each MOSFET explicitly, that produces the same function using only 8 MOSFET's. (Hint: remove the redundancy in the transmission gate drive inverters.)
(c) Draw a complete circuit schematic, detailing each MOSFET explicitly, that produces an exclusive NOR (XNOR) function, using only 8 MOSFET's. The XNOR function is also called the equivalence function.
(d) Question for experts: Draw a complete circuit schematic, detailing each MOSFET explicitly, that produces an XOR function using only 6 MOSFET's total. This is a rather tricky one, but nonetheless a common building block for CMOS logic circuits.

Procedure 11 Flying capacitor voltage inverter

Comment

The flying capacitor voltage inverter is used inside many integrated circuits so that they can operate internally with dual power supply voltages but require only a single external power supply. Similar techniques are used inside memory chips such as EPROMS to generate the programming voltages. The principle of operation is based upon charging a capacitor up to the desired voltage magnitude and then switching its connections so that the polarity is reversed and the charge is transferred to a buffering capacitor on the output. This circuit uses the function generator to provide the clock, but this could easily be replaced by an astable multivibrator of the type examined in Experiment 5 to produce stand-alone operation.

Set-Up

Construct the circuit of Fig. E4.11a using the following components:

R1 = 10 kΩ 1/4W 5% resistor
U1 = CD4016B quad CMOS switch
U2 = CD4007 CMOS MOSFET array
C1, C2, C3, C4 = 0.1 μF capacitor

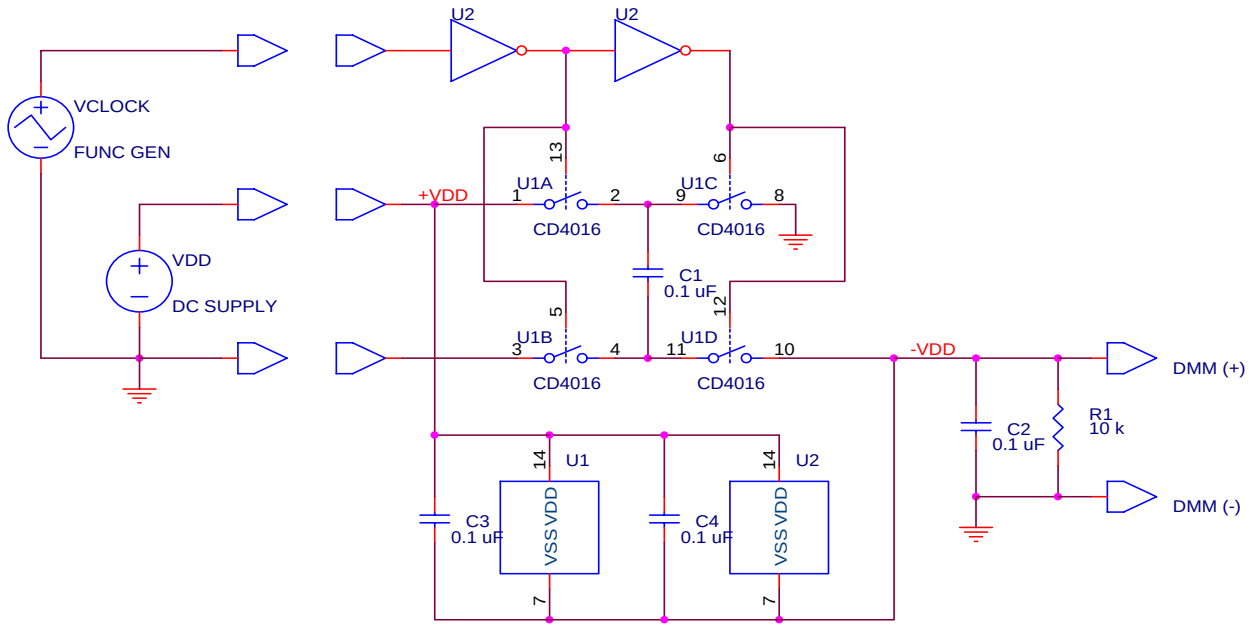

Figure E4.11a

The two logic inverters that drive the analog switches are constructed using the MOSFETs of U2, the CMOS MOSFET array. Their connections are shown in Fig. E4.11b. Another interesting feature of this circuit is that the lower power supply rail that powers U1 and U2 is created by the inverter itself. It is said that the voltage inverter bootstraps its own lower supply rail. The necessity for U1 and U2 to operate from the –VDD supply is because the voltages fed through U1B and U1D would otherwise be lower than the GND

power supply rail and the body diodes of the analog switch MOSFETs would become forward biased, clamping the voltage swing to only that of the power supply rail range. Similarly, the CMOS inverters of U2 must also swing their outputs to –VDD to properly turn on the analog switch MOSFETs of U1.

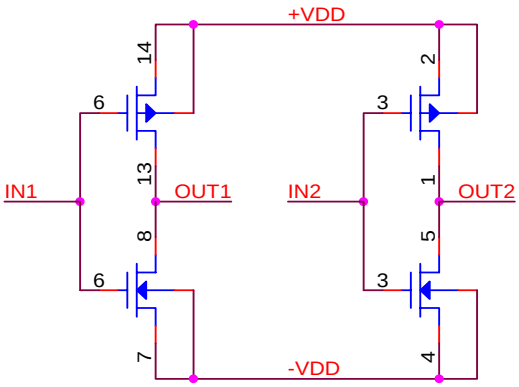

Figure E4.11b

Measurement-11 Connect the circuit as shown above, but leave off R1 for the time being. Set VDD to +5.0 V and configure the function generator to produce a 1 kHz 4.0 V amplitude square wave with a 0.0 V offset. Set a DMM to measure DC volts, and measure the output V_{out}. Vary the frequency of the function generator from 100 Hz to 100 kHz and note any frequencies at which the output voltage changes.

Add the load resistor R1 to the circuit and repeat the above measurements.

Question-11 To better understand the operation of this circuit, it might prove helpful to examine the voltages on both sides of C1 and –VDD versus time for a few clock cycles.
(a) Using a few well chosen sentences, explain why the output voltage drops in magnitude when the load resistor is added.
(b) Using a few well chosen sentences, explain why the output voltage is restored when the clock frequency is increased.
(c) Design a circuit based upon the same principles that outputs a voltage of approximately +2VDD.

Procedure 12 Voltage step-up switch-mode power supply

Comment

This circuit is a very common power supply topology that is used in constructing light weight power supplies for computers and other consumer products. It can produce a wide range of voltages, both greater than and less than the incoming power feed. Unlike the flying capacitor technique, it is not constrained to produce only a integer multiple of the power feed voltage. This circuit stores energy in the magnetic flux of the inductor when its end that is connected to the diode is shorted to ground by the FET. When the FET opens this path, the current through the inductor continues by passing through the diode D1 to charge up capacitor C2. Diode D2 acts as a clipper to keep the output voltage at a constant level. An n-channel MOSFET could also have been used to switch the inductor to ground, such as one of the n-channel MOSFETs in the CD4007 array, or a 2N7000.

Set-Up

Construct the circuit of Fig. E4.12 using the following components:

L1 = 100 mH inductor
J1 = MPF102 n-channel JFET
D1 = 1N4148 diode
D2 = 1N4744 15 V zener diode
R1 = 10 kΩ 1/4W 5% resistor
R2 = 100 kΩ 1/4W 5% resistor
C1 = 10 μF electrolytic capacitor
C2 = 0.1 μF capacitor

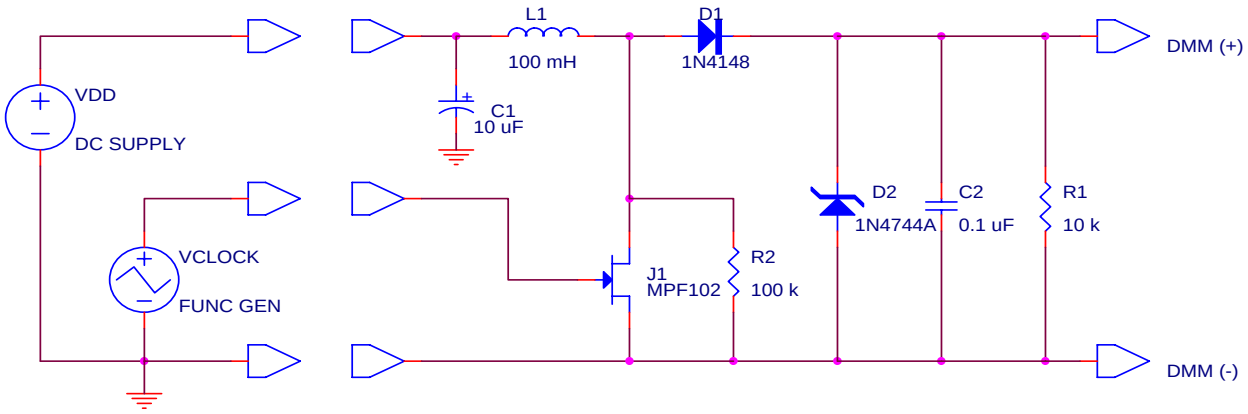

Figure E4.12

Comment

A single transistor in this application makes a better switch than an analog switch. The input supply voltage is always positive, so only an n-channel device is needed. A CD4016B CMOS analog switch would not work in this application because the body diode in the p-channel MOSFET of the switch would clamp the voltage at the node between L1, D1, and J1 to a maximum of VDD + 0.6 V, preventing the circuit from generating any voltages higher than this.

More Set-Up

Construct the circuit as shown, but leave off the load resistor R1 for the time being. Set the input power supply voltage to VDD = +5.0 V and then configure the function generator to produce a 2 kHz square wave that goes between –5.0 V and 0.0 V. Do this by producing a 2.5 V amplitude square wave with a –2.5 V DC offset. This negative voltage is necessary to drive the JFET since the JFET is a D-mode device. (If an n-channel MOSFET were used as the switch, a positive square wave would be needed.) Next, set the duty cycle of the function generator to be 80 %, making the JFET conduct for a longer time than it is turned off.

Measurement-12

Configure a DMM to measure DC volts and measure the output voltage V_{out}. Vary the frequency of the function generator from 100 Hz to 100 kHz and make a note of any frequencies at which the output voltage changes.

Next, add in the load resistor R1 and repeat the measurements and observations of the effect of drive frequency.

Determine what effect R2 has on the circuit by removing it and observing the voltage waveform at the node between L1, D1, and J1 on an oscilloscope.

Question-12

The operation of this circuit can be better understood by examining the voltages on both sides of diode D1 over the span of a few clock cycles.
(a) What is the function of R2?
(b) When the load resistor is added, does increasing the clock frequency help restore the output voltage? Explain why.
(c) Explain why, when the 10 kΩ load resistor is added, the duty cycle for the JFET conduction must not drop below about 80 %.

Procedure 13 Sample and hold gate

Comment

Information signals as well as power can be temporarily held as a charge on a capacitor. An analog switch can be used to transfer a voltage level onto a capacitor and then disconnect it so that the capacitor temporarily stores the voltage, providing a short-term analog memory function. Sample and hold gates are commonly used in analog-to-digital converters (ADCs) to temporarily store the input voltage signal while the digital conversion is taking place.

Set-Up

Construct the circuit of Fig. E4.13 using the following components:

U1 = CD4016B quad CMOS analog switch

C1, C2 = 0.1 μF capacitor

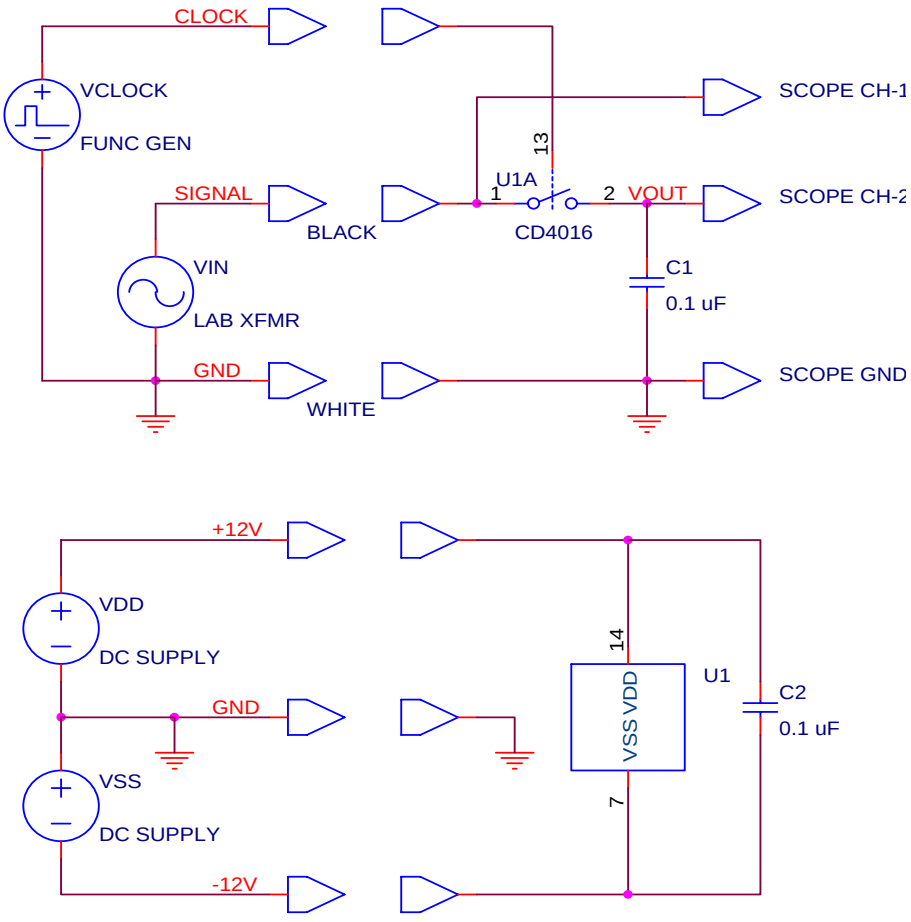

Figure E4.13

Construct the circuit as shown above and configure the function generator to output a 1.2 kHz square wave with an amplitude of 5.0 V and a high time of 20 % of the period. The frequency of the function generator is chosen to be 20 times that of the 60 Hz sinusoid coming from the laboratory transformer. This will cause the analog switch to sample the laboratory transformer signal

20 times per one of its cycles. Configure the DC power supplies to produce ±12 V and connect this to power up the CD4016B.

Measurement-13 Display both the input and sampled versions of the laboratory transformer sinewave on an oscilloscope and print out the display for inclusion in your laboratory notebook.

The sampled signal V_{out} has a step-like nature with each step having a sample phase of 167 μs when the analog switch is closed and a hold phase of 667 μs when the analog switch is open. The sample phase of each step further consists of an acquire phase and a track phase. The acquire phase begins when the analog switch closes and the capacitor charges up to the same voltage as what is being applied at the input. The track phase follows this in which the capacitor charges and discharges through the closed analog switch as necessary to match to the applied input voltage waveform. When the analog switch opens, the capacitor holds the sampled voltage at the value it was at the instant that the switch opened.

The various phases of the output waveform can be viewed by zooming in with the oscilloscope. To do this well, the oscilloscope will have to be accurately triggered. The delaying time base of the oscilloscope can be used to produce the proper delay into the waveform if the trigger signal is obtained from the more slowly varying input sinusoid of the laboratory transformer.

Pick a point on the waveforms in which the output voltage changes appreciably and include in your laboratory notebook a sketch of the input and output voltage waveforms, indicating the acquire, track, and hold phases.

The accuracy of the sampled signal can be improved by increasing the sampling rate. Adjust the frequency of the function generator upwards and examine the output versus input voltage waveforms to confirm this assertion.

Question-13 (a) Using the collected data, estimate the on-resistance of the analog switch. (b) If the on-resistance of the analog switch is $R_{on} = 200\ \Omega$ and the internal resistance of the signal source is $R_s = 50\ \Omega$, what is the maximum rate of change of the input signal (in V/s) for which the maximum error between the input and the sampled signals remains below 5 %?