Experiment-5

CMOS Timing, Logic, and Memory Circuits

Introduction | The objectives of this experiment are to observe the operating characteristics of some CMOS timebase and memory circuits and to gain some practice in the design of CMOS combinatorial and sequential logic circuits.

Precautions | This experiment will use standard 4000-series (JEDEC B-series) buffered CMOS (metal gate) integrated circuits. These IC's have internal diodes to protect the MOSFET gates, but even so, they can still be destroyed by careless handling which may produce stray electrostatic discharge (ESD). Follow the same precautions as for dealing with a discrete MOSFET.

To avoid static discharge damage to the IC, keep the part inserted into black conductive foam whenever it is not being used in a circuit. Alternatively, the pins may be pushed into a small piece of aluminum foil, or the part may be wrapped in the foil, if some conductive black foam is not available. Always discharge any built up static charges from your body by touching a grounded metal object, such as the frame of the lab bench, before handling the IC's. When finished with a given circuit, return the IC to the foam or the foil.

Pay attention so that none of the leads become folded underneath the IC as you press it into the breadboard. If the leads on the IC are bent excessively outward so that they do not fit well into the breadboard, you can make the leads more parallel by rolling the IC on the tabletop to bend all of the leads on one side together.

Exercise the same care when removing the IC from the solderless breadboard. Often, the IC may be held quite tightly by the breadboard, making removal difficult. Use a small screwdriver blade to pry the IC up from underneath in this case. If you choose to use just your fingers to pull the IC from the breadboard, be carefull that the IC does not flip around and stick its sharp leads into your finger. While humans normally kill IC's with static discharges, IC's themselves can bite back in this manner! (Usually this is non-fatal.)

Procedure 1   NAND and NOR gate truth table verification

Set-Up   Configure a DC power supply to output +5.0 Volts and verify this output with a bench DMM. Attach a lead to each output terminal.

Insert a CD4001B (quad 2-input NOR gate) and a CD4011B (quad 2-input NAND gate) IC into a clear space on the solderless breadboard. With the breadboard groove running from left to right, insert the two IC's so that both indexed ends are towards the left. (The indexed end is the one with the dot, depression, or D-shaped cutout which identifies the pin 1 end of the package.) You will use the upper continuous line of tie points on the breadboard for the VDD = +5.0 Volt power supply bus, and the lower continuous line of tie points on the breadboard for the GND = 0.0 Volt power supply bus. For each of the two IC's use a jumper to connect pin 7 to the lower GND bus, and pin 14 to the upper VDD bus. Finally add two 0.1 µF ceramic disk capacitors between the VDD and GND power supply rails. Place one each of these capacitors close to the vicinity of each of the two IC's on the solderless breadboard. These ceramic disk capacitors are non-polar and may be installed in either direction.

Comment   The purpose of these 0.1 µF ceramic disk capacitors is to reduce switching noise in the circuit, also termed "power supply decoupling." This is standard practice for any type of logic family, although it becomes more critical with bipolar logic such as TTL, which produces large current spikes when it switches. CMOS produces less severe current spikes, yet it must still use decoupling capacitors. The capacitors keep the power supply voltage from being pulled excessively downward by switching currents from any nearby IC. Thus, these capacitors should be distributed uniformly about the gates in a digital system. A single large capacitor across the power supply rails in one location does not provide adequate protection against this type of coupling through the power supply bus. For both TTL and CMOS, good design practice is to use one decoupling capacitor for each IC, typically from 0.01 µF to 0.1 µF in value. Many IC manufacturers suggest using less, but usually the cost of a small capacitor of this value range is not a strong function of the capacitor's value. Hence, it costs just as much to use a 0.1 µF as it does to use a 0.01 µF, so one rarely loses by adding more decoupling capacitance.

Comment   Typical small-scale integration (SSI) level circuits contain several gates of the same type in order to fill-out a typical 14- or 16-pin DIP package. For example the CD4001B IC contains four 2-input NAND gates, each of which are identical. Any of the four can be used interchangeably. A consequence of this packaging strategy is that in order to get one, you have to buy four. Obviously, one cannot buy one gate for 1/4 of the price of the IC. These considerations have a strong bearing upon how one designs with SSI-level parts in order to minimize both circuitry and cost. The arrangement of the

gates within the package, i.e. the "pin-out" of the package for the CD4001B IC is shown in Fig. E5.1a, and the pin-out of the CD4011B is shown in Fig. E5.1b.
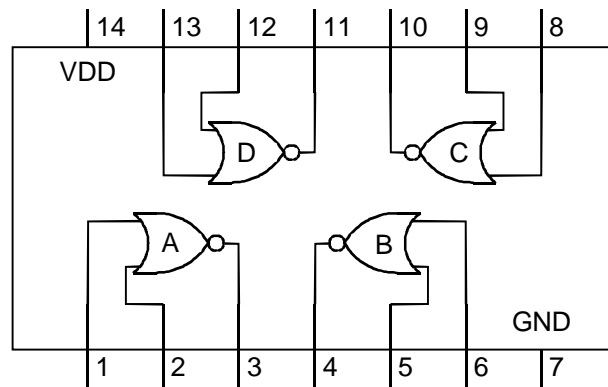

Figure E5.1a   CD4001B Quad 2-input NOR Gate
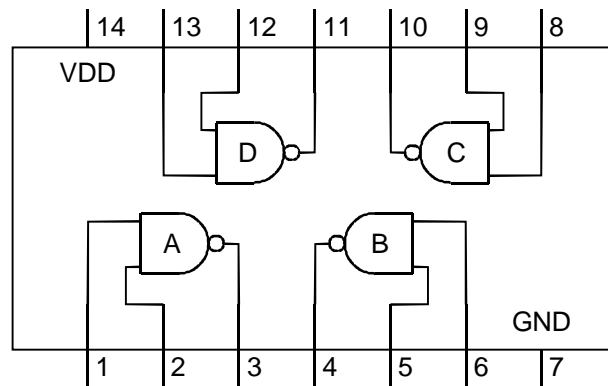

Figure E5.1b   CD4011B Quad 2-input NAND Gate

Comment   The CD4001B, CD4011B, and the CD4016B are examples of homogeneous multipart packages. Each contains multiple parts (four each, denoted A, B, C, and D), and all of the parts are the same. In schematics, the individual parts are laid out using their own schematic symbols (such as the logic symbols shown inside the package frames of Figs. E5.1a and E5.1b) while the power connections to the package are shown elsewhere as a rectangular schematic symbol with only the power pins VDD and GND. Sometimes the package and the power pins are suppressed entirely from the schematic. Separating out the active parts from the power and package overhead allows the schematic to be drawn in a much more logical and meaningful fashion. The CD4007 contains both n-channel and p-channel MOSFETs and is an example of a heterogeneous multipart package. The same schematic layout ideas are usually applied to these parts as well.

Measurement-1   Apply power to the breadboard, connecting the red lead from the positive (+) output of the power supply to the upper +VDD bus, and the black lead from the negative (-) output of the power supply to the lower GND bus.

First you will verify the truth table for the CD4001B NOR gate. Connect a red T-1 LED between the output of the first NOR gate (pin 3) and the lower GND power supply rail. Connect the cathode of the LED to the GND rail. (The cathode lead of the LED is the shorter one, or equivalently, the lead which comes from the side of the plastic dome with a flat on it.) Connect two 2-inch long #22 AWG solid jumper wires to the two inputs of the first NOR gate (pins 1 and 2). Successively connect each of the two input leads to either the VDD or GND power supply rails and record the state of the LED.

Next you will verify the truth table for the CD4011B NAND gate. Connect the red T-1 LED between the output of the first NAND gate (pin 3) to the lower GND power supply rail. Connect the cathode of the LED to the GND rail. Connect two 2-inch long #22 AWG solid jumper wires to the two inputs of the first NAND gate (pins 1 and 2). Successively connect each of the two input leads to either the VDD or GND power supply rails and record the state of the LED.

Question-1   In your notebook construct the truth tables for both the CD4001B NOR and CD4011B NAND gates. Each truth table should include all four possible input combinations.

Comment   Normally, to drive an LED from a voltage source would require the use of a current limiting resistor which would be placed in series with the LED. Such resistors, typically 150 Ω to 470 Ω, are used with open-collector TTL gates to drive standard T-1 and T-1 3/4 LEDs at their recommended 10-20 mA. With CMOS logic these current limiting resistors are not necessary. When the CMOS gate is in either its HIGH or LOW output state, only one transistor of the output buffer is turned on. Suppose that the upper p-channel MOSFET is turned on, as if the gate were outputing a logic HIGH level. Running current through an LED to ground will clamp the output voltage to the turn-on voltage of the LED, typically only 1.5 V or so. Hence, the LED will prevent the output from obtaining a satisfactory HIGH voltage, yet the p-MOSFET will also be clamped into saturation by the LED, which then sets the current flow through the LED to be the saturation current of the p-channel MOSFET. This saturation current is approximately 1 mA for 4000-series CMOS logic (operating at VDD = 5 V), so there is sufficient current to dimly light up the LED and yet it remains limited to this saturation value so there is no danger of burning out the LED with excessive current (as would be the case in TTL logic if the limiting resistor were omitted). To summarize, one can always drive at least one LED (albeit dimly) from a single buffered CMOS output, using either power supply rail. However, when an LED is attached as a load to the CMOS output, that output is no longer usable as a logic input for

driving other CMOS gates. This aspect will be exploited several times in the following procedures.

Procedure 2   Manual combinatorial logic analyzer using LabVIEW

Comment   Simple combinatorial logic circuits can often be tested by hand as was done in the previous procedure. However, as the number of inputs grows, this process can become quite tedious to do exhaustively. In this and the next procedure, two LabVIEW combinatorial logic analyzers will be used to exhaustively test a logic circuit and demonstrate how the process of logic testing can be sped up.

Set-Up   The DC power supply used in the previous procedure can be disconnected and turned off. This and the next procedure will use the digital +5 Volt power that is supplied from the DAQ card to power up the ICs. Keep the CD4001B and CD4011B ICs plugged into a clear area of the solderless breadboard. They will be connected by jumper wires to the DAQ card connector block.

Launch LabVIEW 7.1 from a lab bench computer and open the file ManualCombinatorialLogicAnalyzer.vi. The front panel of this instrument should appear as shown in Fig. E5.2a below.
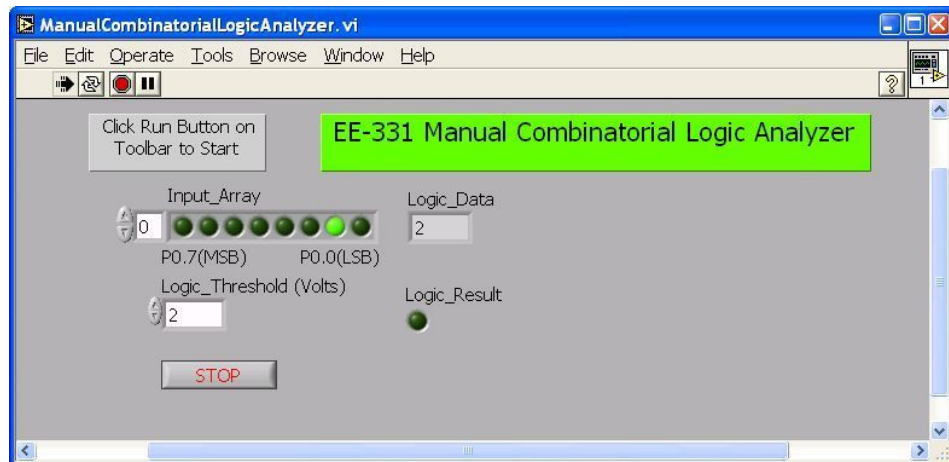

Figure E5.2a

This VI uses the DAQ card digital I/O port to output a logic pattern to the circuit under test (CKTUT), and then uses an analog input channel (AI-0) to read the voltage at the output of the circuit. If the voltage is greater than the Logic_Threshold, it is interpreted as a logic HIGH or "1" state, and the Logic_Result LED is turned on (bright green color). Typically, the Logic_Threshold will be set to about half of the power supply voltage. Up to eight bits can be output simultaneously from this VI using the eight bits of digital I/O on port-0 of the DAQ card. These are named P0.7 through P0.0, with P0.7 being the most significant bit (MSB), and P0.0 being the least significant bit (LSB). Once the VI is running, the output bits can be turned on and off by simply using the mouse to click on the LEDs of the Input_Array. The corresponding LED will light up or extinguish, allowing you to keep track of what logic pattern is being output to the CKTUT. The Logic_Data is

a numerical value of the bit pattern. For example, if the Input_Array were set to 00000010, this would give a Logic_Data value of 2. With 8 bits, the Logic_Data values range from 0 to 255.

Next, connect either a CB-68LP or a CB-68LPR connector block to the 68-wire cable coming from the DAQ card. The pin assignments that will be used on the connector block are as follows:

MSB	P0.7	pin #48
	P0.6	pin #16
	P0.5	pin #51
	P0.4	pin #19
	P0.3	pin #47
	P0.2	pin #49
	P0.1	pin #17
LSB	P0.0	pin #52
DGND		pins #50, #53, #12, #13, #15, or #18
+5V		pins #14 or #18
AI-0		pin #68
AI-GND		pin #67

First connect the analog and digital grounds together using a wire between pins #67 and #12, as shown below in Fig. E5.2b (orange wire). Next, run 6-8-inch long jumper wires from the connector block to the solderless breadboard for the digital I/O outputs, +5V and DGND power, and the analog input. In Fig. E5.2b, +5V is the red wire on pin #14, DGND is the black wire on pin #13, the first four digital logic outputs are white on pin #52, brown on pin #17, blue on pin #49, green on pin #47, and the analog input is the yellow wire on pin #68.
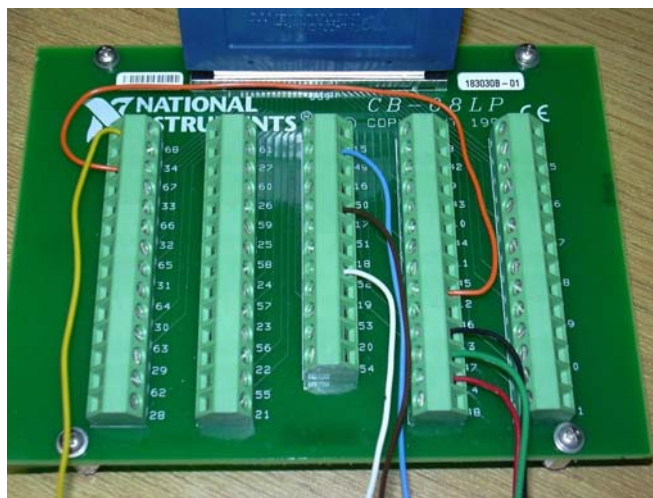

Figure E5.2b

Connect the +5V digital logic power to pin 14 and the DGND digital ground to pin 7of the CD4001B quad 2-input NOR gate. To test the first NOR gate of this IC, gate-A in Fig. E5.1a, connect the P0.0 and P0.1 digital outputs to pins 1 and 2 of the IC, and then connect the analog input AI-0 to the output of the IC on pin 3.

Measurement-2   Click the run button on the toolbar to start the logic analyzer, and enter a Logic_Threshold of 2.0 Volts. Use the mouse to click the P0.0 and P0.1 bits through the four possible combinations and record the state of the Logic_Result LED in your notebook as a truthtable.

Repeat this process using the A-gate of the CD4011B quad 2-input NAND gate and record a truthtable in your notebook.

When done, click the STOP button to halt the VI.

Question-2   Do the truth tables recorded with the LabVIEW logic analyzer agree with those taken manually in Procedure 1?

Comment   You should find that it is quicker and more convenient to use this type of logic analyzer than to manually move the wires around by hand, as was done in Procedure 1.

You might also type Ctrl+E to view the block diagram for the manual combinatorial logic analyzer and observe how simple its structure is.

Procedure 3   Automatic combinatorial logic analyzer using LabVIEW

Comment   If you are continuing on from Procedure 2, you can leave the DAQ card
connector block set up exactly as it was; no changes in the wiring are needed.

Set-Up   Launch LabVIEW 7.1, if it is not already running, and open the
AutomaticCombinatorialLogicAnalyzer.vi. The front panel should appear as
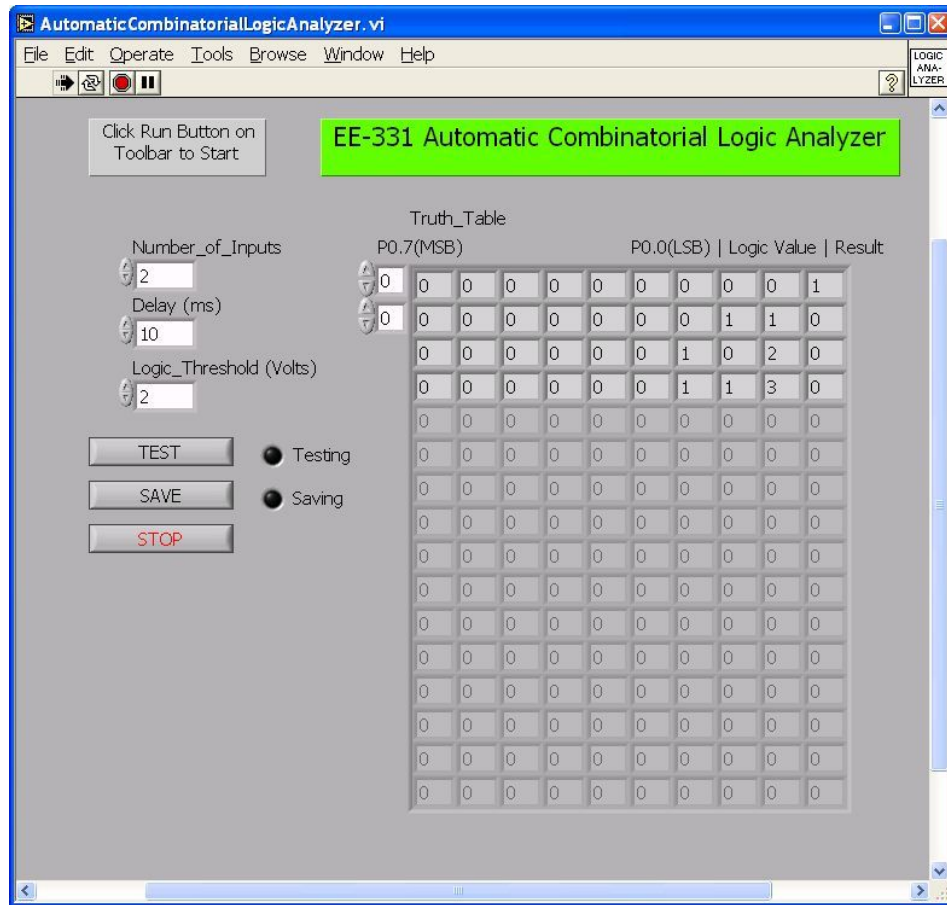shown in Fig. E5.3a below.

Figure E5.3a

This instrument performs the same tests as the manual logic analyzer of
Procedure 2, but it runs through all of the possible digital test patterns
automatically and records the results in its own Truth_Table which is
displayed on the front panel. The Number_of_Inputs (N) is set to be 1 to 8,
from which all 2^N possible logic patterns will be tested. The Delay (ms) is the
amount of time that the instruments waits between sending a new digital test
pattern and reading the analog input from the circuit under test (CKTUT)
output. Logic_Threshold (Volts) is again the voltage level which determines
whether the analog input will be interpreted as a logic "0" or "1". The
Truth_Table shown in Fig. E5.3a has 10 columns. The left-most eight
columns show the individual bit states of the test pattern and the ninth column

shows the equivalent Logic_Value as an integer. The Logic_Result appears in column 10 on the right. The VI is set up by default to show only the first 16 tests, but with 8 bits, up to 256 tests could be performed at a time. To see the other test patterns and results, you can use the upper scroll box on the window.

The DAQ card should be connected to either a CB-68LP or a CB-68LPR connector block using the 68-wire cable. The connector block should then be wired up the same as was done in Procedure 2 (refer to Fig. E5.2b).

Connect the +5V and DGND digital power leads to a CD4001B quad 2-input NOR gate that is plugged into a solderless breadboard. Then connect the first two digital outputs P0.0 and P0.1 to pins 1 and 2 of the IC. Connect the analog input AI-0 to the output of the IC on pin 3.

Measurement-3a Click the run button on the toolbar to start the logic analyzer. Enter 2 for the Number_of_Inputs, a Delay of 10 ms, and a Logic_Threshold of 2.0 Volts. Click the TEST button, and the VI should return with the Truth_Table shown in Fig. E5.3a. You can record this Truth_Table by next clicking on the SAVE button. This will open a window which will allow you to specify the filename and location of an Excel spreadsheet file. The spreadsheet file will be filled with a truthtable identical to that shown on the front panel of the VI.

More Set-Up Now, use the automatic combinatorial logic analyzer to test a more complex logic circuit. Using one CD4011B quad 2-input NAND gate, connect the circuit shown in Fig. E5.3b below:
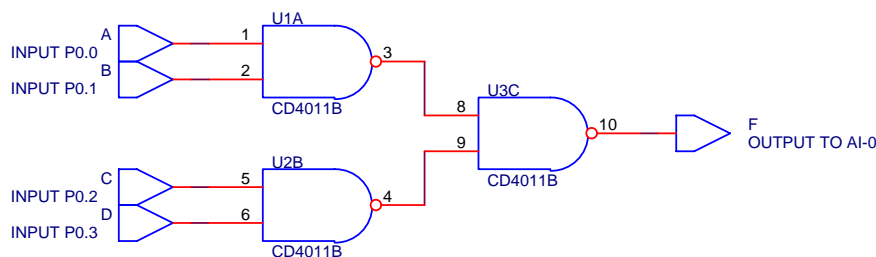
Figure E5.3b

Wire up the first four digital pattern bits {P0.3, P0.2, P0.1, P0.0} to the four inputs marked {A, B, C, D}, and then wire the output marked {F} to the analog input AI-0 of the DAQ card.

Measurement-3b Increase the number of inputs to 4 and click the TEST button on the VI to start the measurement of the 16 digital test patterns. Click the SAVE button and store the resulting truthtable as a spreadsheet file. When finished, click the STOP button to halt the VI. The resulting truthtable should look like that shown in Fig. E5.3c below.
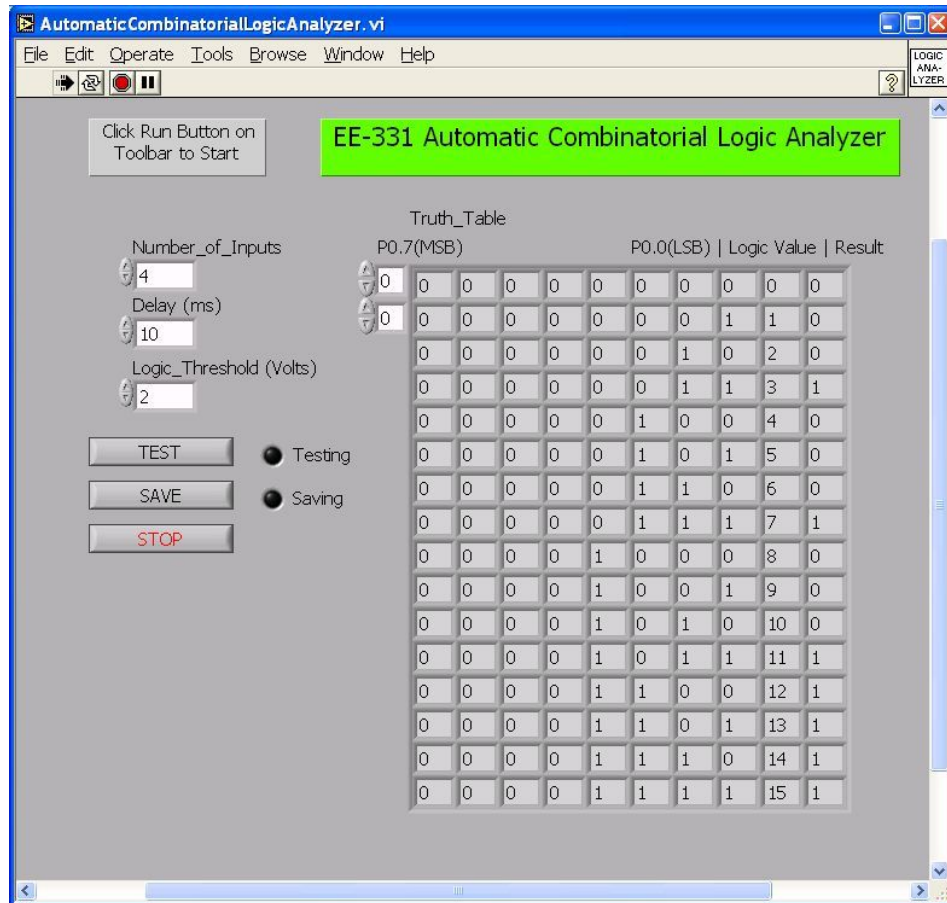
Figure E5.3c

Question-3   From the truthtable that was saved to the spreadsheet file for the circuit of Fig. E5.3b, use a Karnaugh mapping technique to find a simple expression for the logic function that the circuit implements. Express your answer as a simple F = f(A,B,C,D) Boolean function.

Comment   This automatic combinatorial logic analyzer is a very useful tool for testing and debugging digital systems. It is a very simple version of what is found on many more complex commercial logic analyzer instruments, although this simple version does not perform any timing analysis. You may find this VI a useful one to use for troubleshooting other hardware design projects. As you can see, the automatic version of the logic analyzer can save a huge amount of time in digital testing.

Procedure 4   Non-latching monostable circuit

Set-Up   Disconnect the solderless breadboard from the power supply and the DAQ
               card, remove all of the jumper wires and LEDs, but keep the CD4001B and
               CD4011B ICs still plugged into the breadboard. Connect the circuit shown
               below in Fig. E5.4 using the following parts:
               C1 = 0.1 μF
               C2 = 0.1 μF
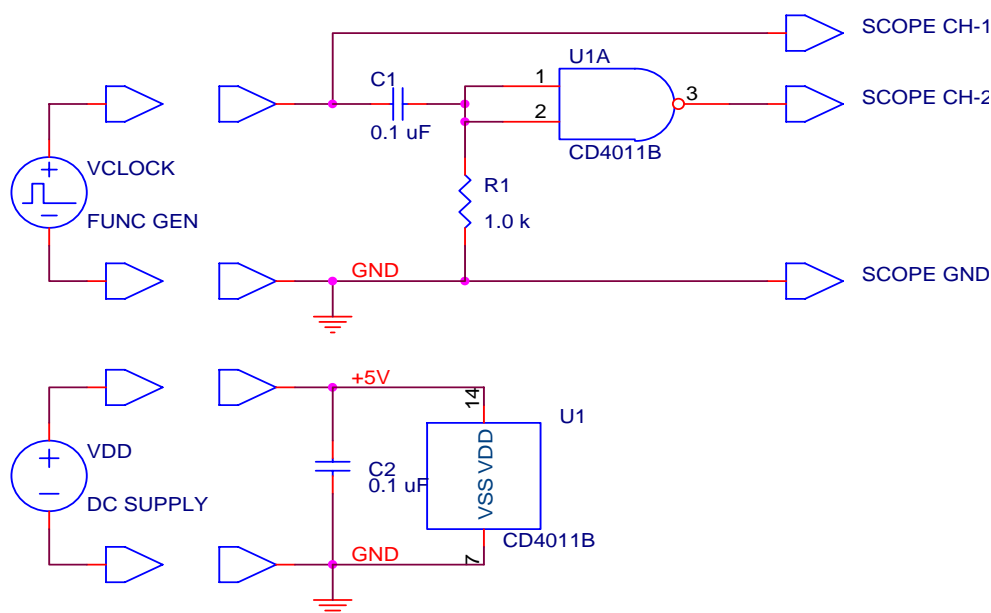   R1 = 10 kΩ 5% 1/4 W
               U1 = CD4011B

Figure E5.4

Use two jumper wires to connect pin 14 of the CD4011B IC to the VDD bus
and pin 7 to the GND bus of the breadboard. Note that the first NAND gate
(the "A" gate) of the CD4011B IC is connected to function as an inverter gate.

Configure a function generator to output a square wave of 1 kHz frequency
which makes transitions from a maximum voltage of +5.0 V to a minimum of
0.0 V. You will normally have to piddle with the amplitude and DC offset
controls to produce this type of waveform.

Connect a 10× oscilloscope probe to the BNC connectors of both Ch-1 and
Ch-2 of an oscilloscope, configure the vertical mode to CHOP, and set the
vertical scale factors for both channels to 5 V/div with DC coupling. Set the
horizontal timebase to 1 ms/div and set the trigger source to Ch-1 with
positive edge triggering and DC coupling. Use the position controls to put the
Ch-1 trace in the upper half of the screen and the Ch-2 trace below it in the

lower half of the screen. This configuration of the oscilloscope will be used for Procedures 4-6.

Connect the output of the function generator to channel-1 of the oscilloscope and verify that the output of the function generator is correct.

Measurement-4　Connect the power supply leads to the breadboard and connect the output of the CD4011B gate (pin 3) to channel-2 of the oscilloscope. Apply the output of the function generator to the capacitor as shown in Fig. E5.2. The oscilloscope should show a *negative-going* output pulse which is initiated by the *rising* edge of the input square wave.

Use the oscilloscope to determine the width of the output pulse. You may have to readjust the time base of the oscilloscope for this. Now change the frequency of the input square wave to 10 kHz. Remeasure the width of the output pulse. Adjust the frequency of the function generator up and down to determine the range of frequencies for which the circuit still produces an output pulse of fixed time duration.

Change the value of R1 from 10 kΩ to 33 kΩ. Remeasure the width of the output pulse and verify that it is still independent of the input frequency.

Question-4　The width of the output pulse is given by T = kR1C1, where k is a dimensionless constant. Determine the constant k for the above circuit.

Comment　This circuit is termed a non-latching monostable because the input trigger pulse must remain HIGH for a time at least equal to the output pulse width T in order for the circuit to produce an output pulse whose width is T. If the input trigger pulse goes LOW before the monostable has cycled through, then the output pulse will be prematurely terminated at a width of less than T. Thus, this circuit only becomes useful if one wants an output pulse which is *shorter* in duration than the trigger pulse. However, this circuit would also be termed a "retriggerable" monostable, since it will output pulses just as fast as they can be triggered at the input, even if they do not get to take on their full duration. This sometimes has advantages when pulses must be counted without missing any.

Procedure 5   *Latching monostable circuit*

Set-Up   Temporarily disconnect the power supply, function generator, and oscilloscope from the breadboard, and simply modify the circuit of Procedure 4 to add an additional 2-input NAND gate to the input of the monostable, as shown in Fig. E5.5 below. Use the following parts:

       C1 = 0.1 μF
       C2 = 0.1 μF
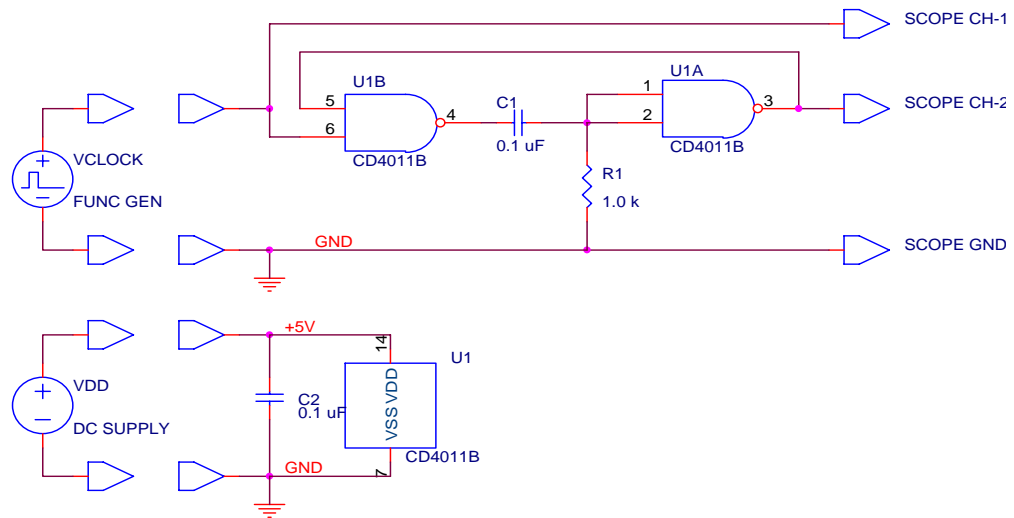   R1 = 10 kΩ 5% 1/4 W
       U1 = CD4011B

Figure E5.5

After carefully checking your circuit connections, connect the power supply to the breadboard, connect the function generator output to the input, the oscilloscope Ch-1 to the input, and the oscilloscope Ch-2 to the output, as shown in Fig. E5.5.

Measurement-5   The oscilloscope should again show a *negative* output pulse which is now initiated by the *falling* edge of the input square wave. Measure the width of the output pulse. You may have to adjust the oscilloscope time base in order to get an accurate measurement.

Increase the frequency of the function generator output up until the point where the period of the input square wave is nearly equal to the width of the output pulse. You should note that the circuit continues to produce the proper output pulse without the "recovery time" that the non-latching monostable of Procedure 2 required.

Question-5   (a) The width of the output pulse is again given by $T = kR1C1$, where k is a dimensionless constant. Determine k for the above circuit.

(b) Comment on the differences between non-latching and latching monostable circuits.

(c) In your notebook, draw the schematic for a latching monostable circuit which produces a *positive* output pulse which is initiated by the *rising* edge of an input trigger pulse. Label all ICs and give pin numbers to each gate input and output.

Comment   This is circuit is termed a "latching" monostable because the output pulse is fed back to the first (B) gate and has the effect of blocking any new trigger pulses that may occur until the monostable has completely cycled through its output pulse of width T. Hence, this circuit may be used to output pulses which are either *shorter or longer* than the input trigger pulse. This circuit would also be termed "non-retriggerable" since the input is disabled while the output pulse is present.

Procedure 6   CMOS square wave oscillator

Set-Up

Disconnect the power supply, oscilloscope probes, and function generator leads from the breadboard, remove all resistors, capacitors, and jumper leads, but leave the CD4001B and CD4011B ICs still plugged in. Construct the circuit of Fig. E5.6 below using the following parts:

R1 = 10 kΩ 5% 1/4 W
R2 = 100 kΩ 5% 1/4 W
C1 = 0.047 µF
C2 = 0.1 µF
U1 = CD4001B or CD4011B ***
*** choose whichever you prefer since they are connected as inverters.
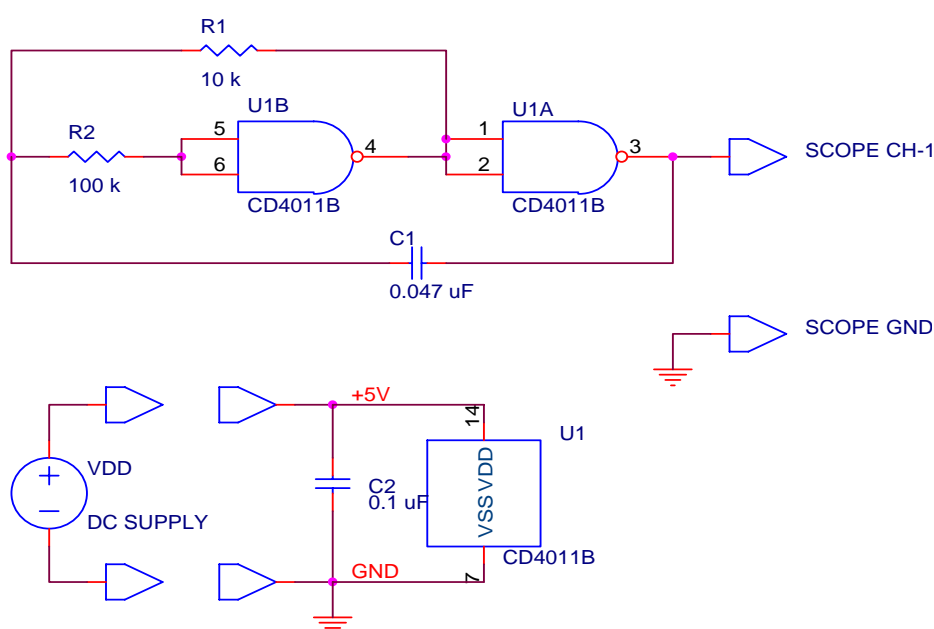

Figure E5.6

Implement the two inverters of Fig. E5.6 using gates A and B of either the CD4001B quad NOR IC or the CD4011B quad NAND IC. Use the pin-out diagrams of Figs. E5.1a and E5.1b to determine the correct pin numbers to use.

After carefully checking your circuit connections, connect the power supply to the breadboard and connect Ch-1 of the oscilloscope to the output. (This circuit is an oscillator and does not require any input signal.)

Measurement-6

Adjust the time base of the oscilloscope to display the output of the oscillator circuit. Measure the period of the waveform, make a sketch of the waveform in your notebook, and measure the symmetry of the waveform, i.e. the ratio of the HIGH time to the LOW time.

Replace resistor R2 with a value of 1.0 kΩ 5% 1/4W. Re-examine the output waveform and note any differences from the previous case.

Question-6   (a) The period of the output waveform is given by $T = kR1C1$, where k is a dimensionless constant. Determine k for the above oscillator circuit.
(b) Comment whether R2 has any effect on the frequency of the output waveform. Does R2 have any effect on the output waveshape?
(c) Question for experts: Speculate on the purpose of R2. Hint: Remember that the inputs to the CD4000B series ICs have input protection diodes.

Procedure 7   Logic function implementation design

Set-Up   Disconnect the power supply and oscilloscope probe(s) from the breadboard; however, leave the CD4001B and CD4011B ICs still plugged in.

Design-7   Using only the one CD4001B quad 2-input NOR gate and the one CD4011B quad 2-input NAND gate which are presently plugged into the solderless breadboard, design a circuit to implement the following logic function:
$$F = f(A,B,C) = (A \oplus B)C,$$

where $\oplus$ indicates the exclusive-OR function.

Feel free to use DeMorgan's Theorem, or any other Boolean logic manipulations, to rearrange the logic expression into a more convenient form, if necessary.

Construct the circuit that you designed using only the CD4001B and CD4011B ICs. Connect a red T-1 LED between the output terminal and ground to monitor the output state, and use three 2-inch long #22 AWG jumper wires to connect the A, B, and C inputs to either VDD or GND. Be sure to connect the cathode of the LED to the GND rail.

Measurement-7   After carefully checking your circuit connections, connect the power supply leads to the breadboard and test all of the possible input combinations to produce a truth table for the circuit. Alternatively, you may wish to use the automatic combinatorial logic analyzer of Procedure 3 to test your circuit design.

Question-7   Record the truth table in your notebook. Does it properly implement the desired logic function? If not, give a reason why, and then redesign the circuit to eliminate the problem.

Procedure 8   Hardwired D-type flip-flop

Set-Up   Disconnect the power supply leads from the breadboard and remove all of the jumper leads, capacitors, and LEDs.   Keep the CD4001B and CD4011B ICs plugged into the breadboard. Construct a D-type flip-flop using four 2-input NAND gates and one 2-input NOR gate (to form an inverter) as shown below in Fig. E5.8. The remaining two 2-input NOR gates in Fig. E5.8 are connected as inverters to buffer the outputs in order the drive the two LEDs. Use the following parts:

$R1 = 10$ kΩ 5% 1/4 W
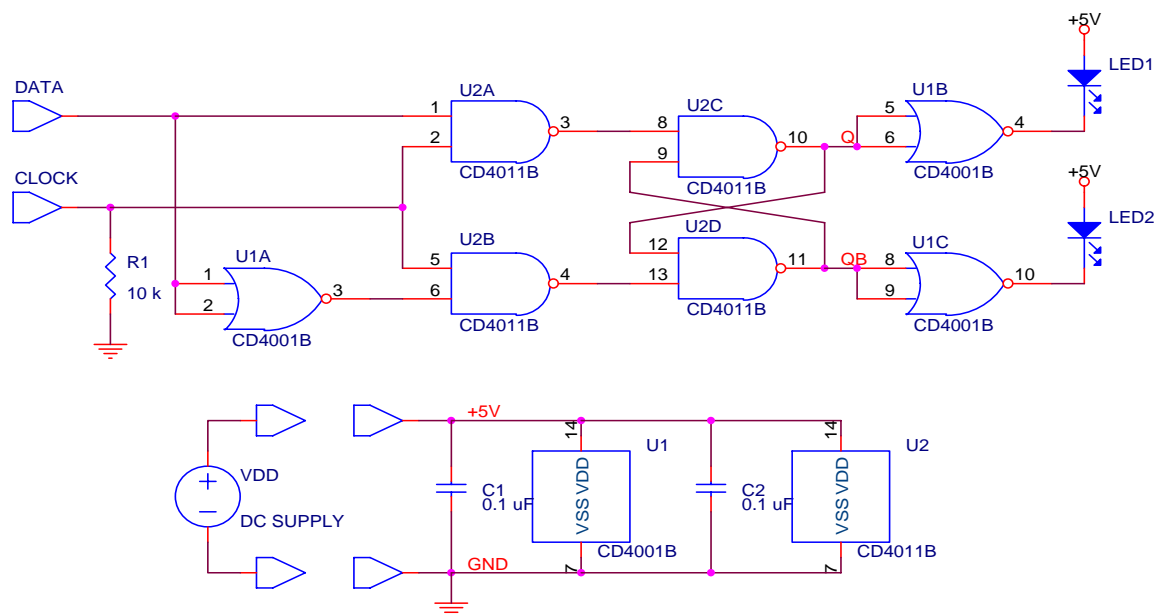C1, C2 = 0.1 μF
U1 = CD4011B
U2 = CD4001B

Figure E5.8

Connect the anode of a red T-1 LED to the two outputs of the flip flop as shown in Fig. E5.8. Also connect a $R1 = 10$ kΩ pull down resistor to the clock input as shown. After re-checking all circuit connections, connect the power supply leads to the breadboard. One of the two LEDs should lite up.

Measurement-8   Use a short 2-inch long jumper wire to connect the D input of the flip flop to the GND rail. Use another jumper to briefly connect the clock input to the VDD rail. This pulse should reset the flip flop so that the Q output is LOW (LED = OFF). Now connect the D input of the flip flop to the VDD rail. Briefly touch the clock input to the VDD rail, and the Q output should go to a HIGH state (LED = ON). Experiment with the D and clock inputs to determine the transition truth table for the D-type flip flop. Record this in your notebook.

Procedure 9   Asynchronous frequency divider circuits

Set-Up   Completely clear all of the existing parts from the solderless breadboard and use two CD4013B dual D-FFs to implement the four flip-flops in the circuit shown in Fig. E5.9. Use the following parts:
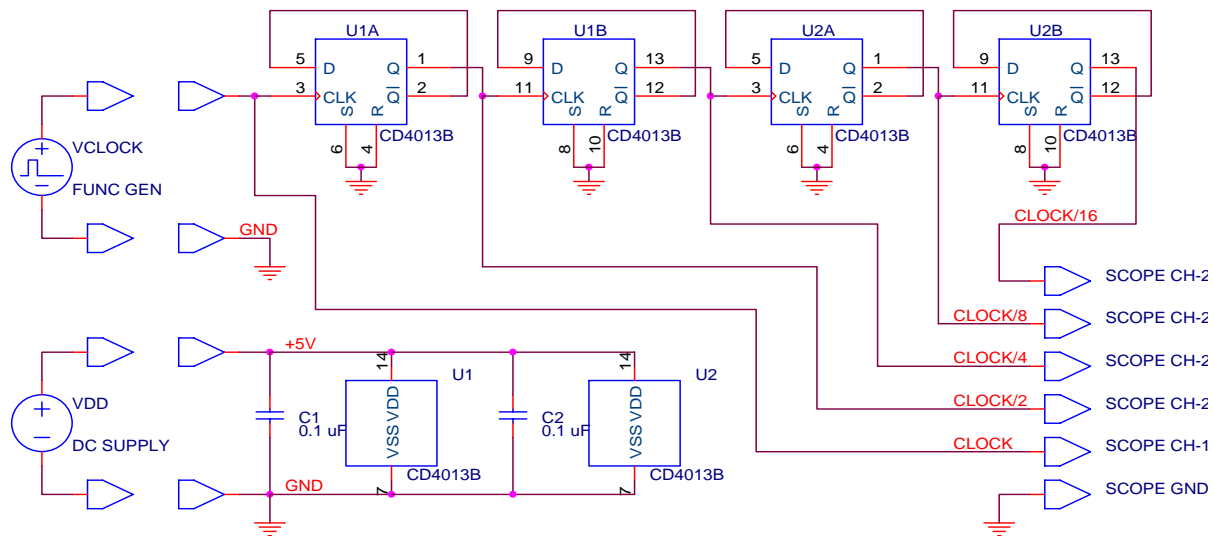   C1, C2 = 0.1 µF
   U1, U2 = CD4013B

Figure E5.9

Note carefully that the SET and RESET (S and R) inputs to each flip flop (pins 4, 6, 8, and 10 on each IC) must be connected to ground. After checking your circuit connections, connect the power supply leads to the breadboard. Configure a function generator to output a 10 kHz squarewave which makes transitions from a maximum of +5.0 V to a minimum of 0.0 V. Apply this input signal to the clock input of the first flip flop, as shown above in Fig. E5.9. Use an oscilloscope to monitor the output of the function generator on Ch-1. Use Ch-2 of the oscilloscope to examine the Q output of each of the four flip flops (one at a time, of course).

Measurement-9   Compare the Q output waveforms from each of the four flip flops to the input signal from the function generator. Use the oscillscope to measure the frequency of both of these outputs. In order to get a stable display on the oscilloscope, you will have to trigger from the lower frequency signal, namely Ch-2. Another way to do this is to use the lowest frequency signal of all, the CLOCK/16 signal from pin 13 of U2B, as an external trigger to the oscilloscope. This will make it easier to see how the various signals relate to one another in time on the oscilloscope. In your notebook draw a timing diagram that contains the input squarewave and each of the four Q-outputs from the D flip-flops.

Question-9 (a) What function is provided by each of the four D-FF circuits?
       (b) Describe how this circuit operates using the transition truth table that you found earlier in Procedure 8.
       (c) Explain why the above circuit would be termed "asynchronous."

Comment   The circuit of Fig. E5.9 is also known as a binary ripple counter.

Procedure 10   Synchronous finite state machine

Set-Up   Disconnect the power supply leads from the breadboard, and remove all of the jumper wires and capacitors. Keep the two CD4013B ICs still plugged into the breadboard. Add a CD4001B and a CD4011B IC to either side of the CD4013Bs on the breadboard. The CD4011B will be used later. Connect the circuit of Fig. E5.10a below using the following components:

R1, R2, R3, R4, R5 = 10 kΩ 5% 1/4 W
C1, C2, C3 = 0.1 µF
LED1, LED2, LED3 = red T-1 LED
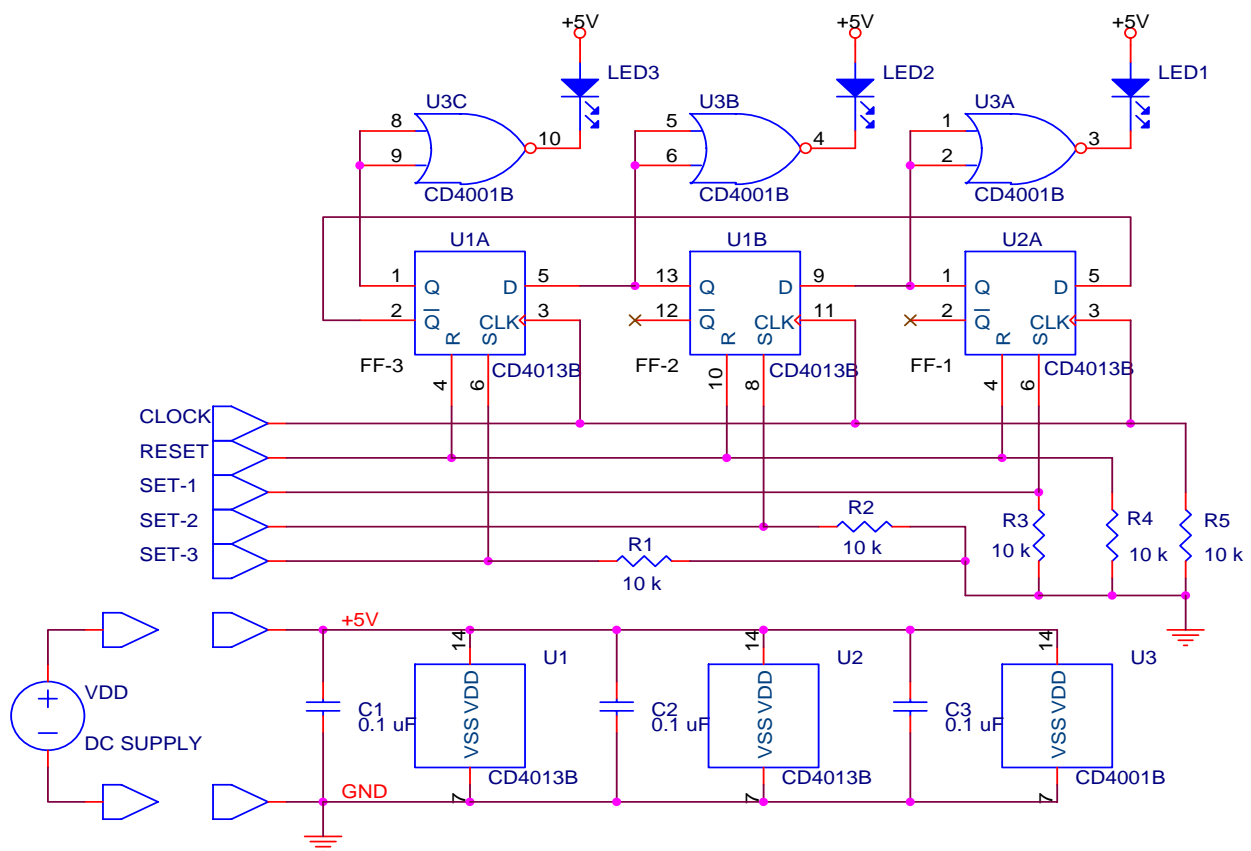U1, U2 = CD4013B
U3 = CD4001B

Figure E5.10a

The three NOR gates from the CD4001B IC are used to buffer the Q outputs of the three D-FFs in order to drive the LEDs. The LEDs will lite when the Q output of their associated FF is HIGH. The five resistors are used to pull the CLOCK, SET, and RESET inputs to a normally LOW level. To pulse any of these five inputs HIGH, briefly touch a wire from the VDD power supply rail to any of the input nodes. Be careful to make the touch very brief and distinct, as you may otherwise introduce bounces which will produce several

pulses instead of just one. This will be particularly noticeable on the CLOCK input, in which bounces may advance the system by several state changes instead of just the desired one.

After checking your circuit, connect the power supply leads to the breadboard. Some of the LEDs may lite.

Measurement-10 Make a table in your notebook, each line of which will contain the bit pattern from each of the three flip flops. If FF-3 is HIGH, FF-2 is HIGH, and FF-1 is LOW, you would record this as the bit pattern 110, or state "6." (Read the three LEDs off in octal code.)

Record the initial state as the first entry in your table. Briefly connect the clock input to the VDD power supply rail. The LEDs should change state. Record this new bit pattern as the second entry in your table. Continue with this procedure until you have mapped out the entire set of states in this circuit. You should be able to predict the next state (following a clock pulse) for each of the eight possible states (0, 1, ..., 7) of the system. You may find that there exist some cycles between states. In order to get to all of the possible states, you should pulse the RESET, SET-1, SET-2, and SET-3 input lines as appropriate.

Question-10 (a) In your notebook, construct the complete state diagram for this circuit, indicating each state by a circle with the state number or bit pattern in it, and drawing an arrow from this state to the next state that would occur following a clock pulse. Be sure to account for all 8 possible states.
(b) What are the cycle lengths of this circuit?
(c) Is the circuit guaranteed to be self-starting? That is, can it be relied upon to always power up into the proper cycle?

Modifications This circuit is supposed to be a 6-state machine which is self-starting, meaning that it does not require any reset pulses to start it off into the proper cycle. A self-starting system (which is highly desirable for robust digital design) is one where all of the states which are not part of the desired cycle at least feed into the desired cycle after a sufficient number of clock pulses. You will now modify the state machine of Fig. E5.10a to be self-starting. Disconnect the jumper wire which connects the D input of FF3 to the Q output of FF2. In its place construct the circuit shown in Fig. E5.10b below which produces a D input to FF3 of D3 = Q1Q2 + Q2Q3. Implement this additional circuitry using three 2-input NAND gates from the CD4011B IC.
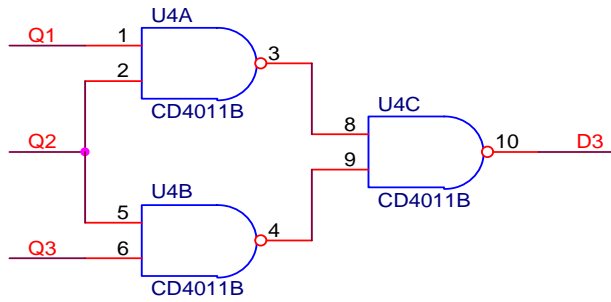
Figure E5.10b

Measurement-10 Make another table in your notebook, each line of which contains the bit pattern from each of the three flip-flops. Pulse the CLOCK line successively to map out the new state that each old state becomes following the clock pulse.

Question-10 (d) Draw a complete state diagram which shows all 8 possible states of the system and draw arrows from state to state to show how each is affected by the clock pulses.
(e) Discuss why or why not this system is now self-starting.

Procedure 11   Push-on/push-off circuit

Set-Up   Disconnect the power supply leads from the breadboard, and remove all of the jumpers and any other components. Keep the CD4011B quad 2-input NAND IC still plugged into the breadboard; the other ICs may be removed. Construct the circuit shown in Fig. E5.11 below using three of the NAND gates on the CD4011B IC to implement the inverters. The purpose of the last ("C") inverter is only to buffer the output in order to drive the LED. The parts are as follows:

> R1 = 4.7 kΩ 5% 1/4 W
> R2 = 220 kΩ 5% 1/4 W
> C1 = 0.05 µF
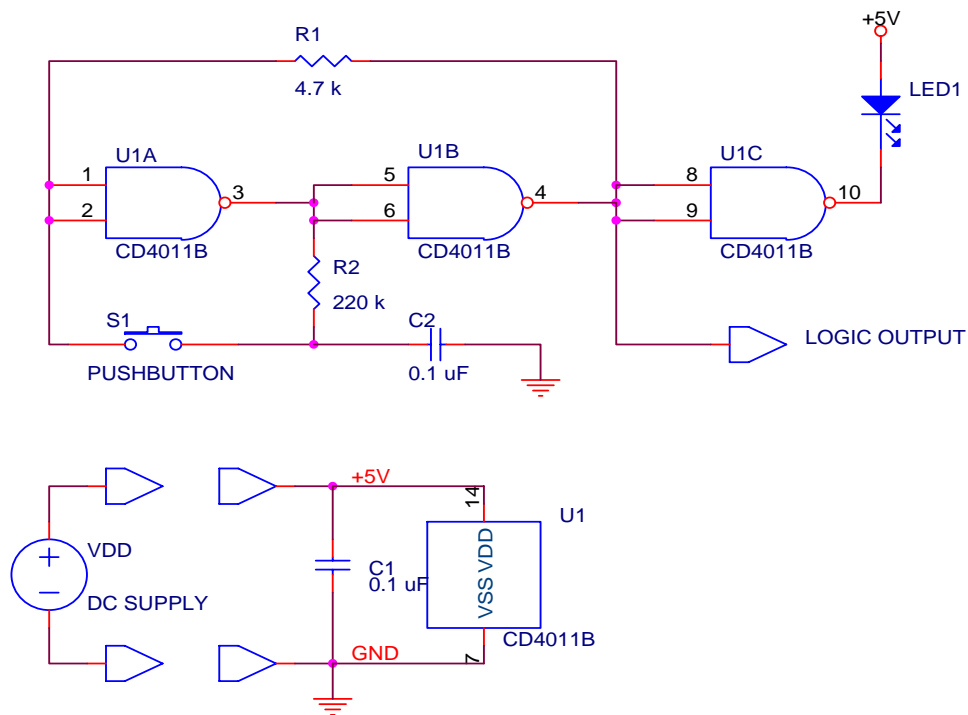> C2 = 0.1 µF
> LED1 = red T-1 LED
> U1 = CD4011B

Figure E5.11

After checking your circuit, connect the power supply leads to the breadboard. Use a short 2-inch long jumper wire to implement the push button.

Measurement-11 Successively touch the jumper wire to the other connection point to simulate a press of the push button and observe the effect on the LED.

Question-11   Question for experts: Explain how this circuit works.

Comment   This circuit is a very compact way to implement a de-bounded push button input to a logic system. It only works with CMOS logic circuits, which gives you at least one clue as to its operation.

Procedure 12   CMOS ring oscillator

Comment   A ring oscillator is a circuit which is used for testing the speed of logic gates.
                An odd number of inverters is connected into a single loop, so that a change in
                logic state continues to propagate around the loop. The period of the resulting
                oscillation is equal to the propagation delay of a single inverter times the
                number of inverters in the loop times two (since the change in state must
                make two complete round trips to restore the system to its starting state). The
                propagation delay of each inverter is determined by its current drive ability
                and the output node capacitance that it must charge and discharge.

Set-Up   Disconnect the power supply leads and clear all parts from the breadboard.
                Use a single CD4001B quad 2-input NOR IC to implement the circuit shown
                below in Fig. E5.12. Notice that each of the NOR gates is connected to
                function as an inverter. Use the following parts:
                    C1 = 0.1 µF
                    C2, C3, C4 = 33 pF, 220 pF, or 1000 pF ***
                    U1 = CD4001B
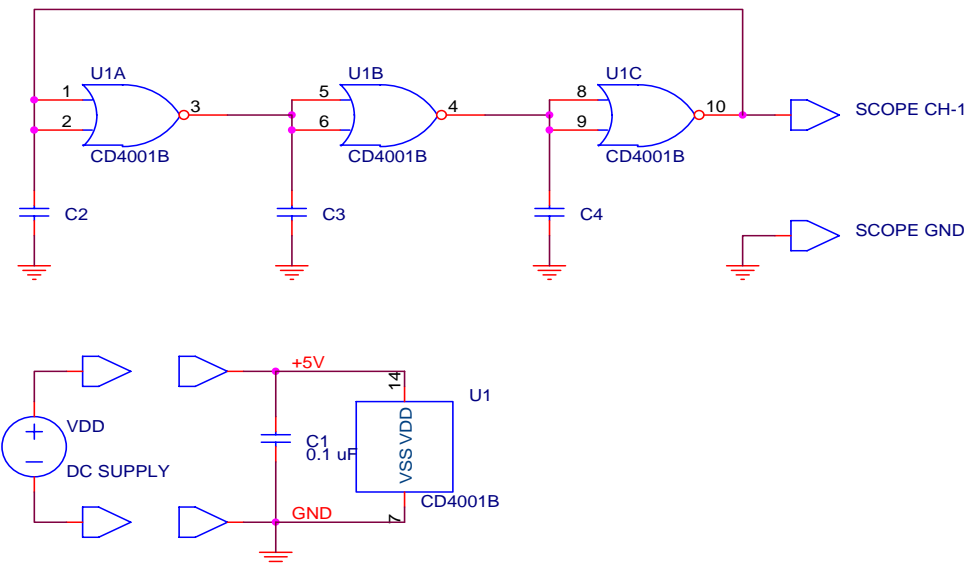   ***initially install a 33 pF capacitor for each of C2, C3, and C4

Figure E5.12

                Connect the output of the ring oscillator to Ch-1 of an oscilloscope using a 10
                × probe. Configure the oscilloscope to display only Ch-1 at 2 V/div. Set the
                triggering to AUTO and the triggering source to Ch-1. You will have to
                experiment with the timebase to fit 2 or 3 complete cycles into the display.

Measurement-12 Apply +5.0 Volt DC power to the breadboard and you should observe a
                waveform on the oscilloscope whose frequency is roughly around 1 MHz.
                The waveform will not look like a pretty square wave, but will have a good
                deal of rounding on its corners. Nevertheless, we shall still refer to this as a

"square wave," its shape notwithstanding. Use the oscilloscope to measure the frequency of the waveform to at least two significant figures.

Next, remove all of the 33 pF capacitors and remeasure the frequency of the waveform, again to two significant figures, if possible.

Next, install 220 pF capacitors to each of the inverter output nodes and remeasure the oscillator frequency. Finally, change the capacitors to 1000 pF and remeasure the oscillator frequency.

Now, change the capacitors back to 33 pF, and increase the DC power supply output voltage to +10.0 Volts. Remeasure the output waveform frequency. Finally, increase the DC power supply output voltage to +15.0 Volts and remeasure the output waveform frequency. Be very careful to not exceed +15.0 Volts on the DC power supply, since much higher than this will destroy the CMOS integrated circuits, which are only rated at +18.0 Volts, absolute maximum.

Question-12   (a) From your measured values of oscillation frequency, calculate the propagation delay of a single inverter for each of the circumstances measured above.
(b) Make a plot of propagation delay versus output node capacitance, noting that an unknown built-in capacitance is present at each node in addition to the capacitors which were intentionally added. From your graph, try to extrapolate what the built-in capacitance of each node is. For simplicity, ignore any capacitance added by the oscilloscope probe.
(c) Make a plot of propagation delay versus power supply voltage. Is this plot more closely linear or quadratic in shape?
(d) Explain why increasing the power supply voltage decreases the propagation delay time.

Comment   Ring oscillator tests, while commonly used to compare logic families, should normally be treated with a good deal of suspicion, because they rarely reflect the conditions that the logic gates will be operating under when in a real circuit application. The ring oscillator test will always produce an optimistic speed for the logic family, because the fan-out of each gate is only one, i.e. the output of a gate drives only one input to another gate. In a more realistic situation, the fan-out will be a good deal greater than this, since one output will typically drive 2-5 inputs. The increased fan-out will increase the output node capacitance, which will in turn increase the propagation delay time for each gate.