Homework 8 Solutions

1. J&B P7.19

(a) Symmetrical CMOS inverter

$$V_{IL} = \frac{1}{4}\left(\frac{3}{2}V_{DD} + V_T\right) = 1.425\ V$$

$$V_{IH} = \frac{1}{4}\left(\frac{5}{2}V_{DD} - V_T\right) = 1.875\ V$$

$$V_{IL} + V_{IH} = 3.3\ V$$

$$V_{OL} = \frac{1}{4}\left(\frac{1}{2}V_{DD} - V_T\right) = 0.225\ V$$

$$V_{OH} = \frac{1}{4}\left(\frac{7}{2}V_{DD} + V_T\right) = 3.075\ V$$

$$NM_L = V_{IL} - V_{OL} = 1.20\ V$$

$$NM_H = V_{OH} - V_{IH} = 1.20\ V$$

(b) CMOS with equal $\frac{W}{L}$ values for the NMOS and PMOS

$$K_R = \frac{K_n}{K_p} = 2.5$$

$$V_{IL} = \frac{2\sqrt{K_R}(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{K_R + 3}} - \frac{(V_{DD} - K_R \cdot V_{TN} + V_{TP})}{K_R - 1} = 1.17\ V$$

$$V_{IH} = \frac{2K_R(V_{DD} - V_{TN} + V_{TP})}{(K_R - 1)\sqrt{1 + 3K_R}} - \frac{(V_{DD} - K_R \cdot V_{TN} + V_{TP})}{K_R - 1} = 1.61\ V$$

$$V_{OL} = \frac{(K_R + 1)V_{IH} - V_{DD} - K_R V_{TN} - V_{TP}}{2K_R} = 0.17\ V$$

$$V_{OH} = \frac{(K_R + 1)V_{IL} + V_{DD} - K_R V_{TN} - V_{TP}}{2K_R} = 3.13\ V$$

$$NM_L = V_{IL} - V_{OL} = 1.00\ V$$

$$NM_H = V_{OH} - V_{IH} = 1.52\ V$$

2. J&B P7.22

Current flows through M_{P1} and M_{N2}, assume both in triode region,

$$I_{DN} = I_{DP}$$

$$K_n'\left(\frac{W}{L}\right)_N\left(V_{DD} - V_{TN} - \frac{1}{2}V_O\right)V_O = K_p'\left(\frac{W}{L}\right)_S\left(-V_{DD} - V_{TPS} - \frac{1}{2}(V_O - V_{DD})\right)(V_O - V_{DD})$$

$$V_O = 0.98\,V$$

Check: $V_{GSN} = 2.5\,V > V_{TN} = 0.6\,V$, $V_{GSN} - V_{TNS} = 1.9\,V > V_{DSN} = 0.98\,V$, NMOS is triode. $V_{GSP} = -2.5\,V < V_{TN} = -0.6\,V$, $|V_{GSP} - V_{TPS}| = 1.9\,V > |V_{DSP}| = 1.52\,V$, PMOS is triode.

$$I_{DN} = I_{DP} = 2.7\,mA$$

3. J&B P7.47

(a)

$$100\,\mu A \cdot V^{-2}\frac{15}{1}(V_{in} - 0.6\,V)^2 = 40\,\mu A \cdot V^{-2} \cdot \frac{15}{1}(3.3\,V - V_{in} - 0.6\,V)^2$$

$$V_{in} = 1.414\,V$$

$$I_{DMAX} = 496.5\,\mu A$$

(b)

$$100\,\mu A \cdot V^{-2}\frac{15}{1}(V_{in} - 0.6\,V)^2 = 40\,\mu A \cdot V^{-2} \cdot \frac{15}{1}(2.5\,V - V_{in} - 0.6\,V)^2$$

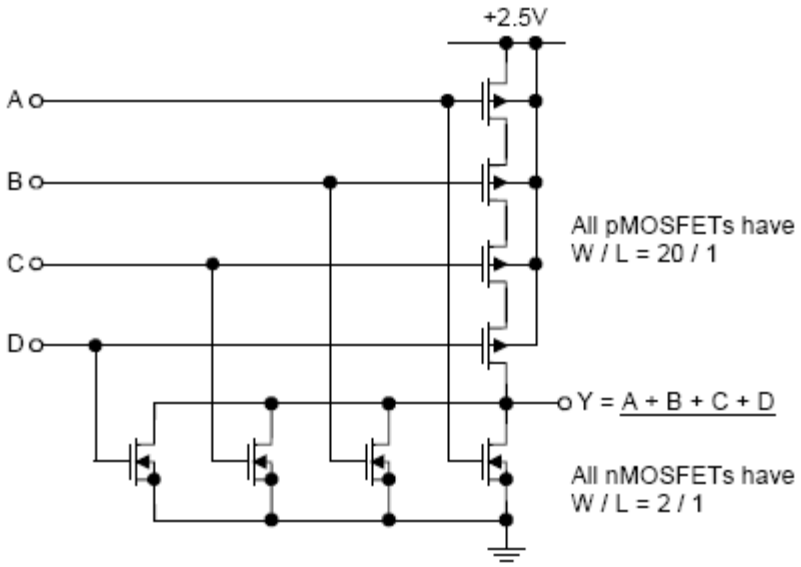
$$V_{in} = 1.104\,V$$

$$I_{DMAX} = 190.3\,\mu A$$

4. J&B P7.62

(a) Since the NMOS devices will be in parallel, their $\frac{W}{L}$ ratios will be same as that in the reference inverter of the figure 7.12 as shown below, or $\left(\frac{W}{L}\right)_N = \frac{2}{1}$. The PMOS devices will be series, however, so their $\frac{W}{L}$ ratios will be multiplied by 4 from the reference inverter of the figure 7.12, or $\left(\frac{W}{L}\right)_P = 4 \times \frac{5}{1} = \frac{20}{1}$.

(b) To drive three times the load capacitance with the same propagation delay, the $\frac{W}{L}$ ratios for each device must be increased by a factor of three: $\left(\frac{W}{L}\right)_N = \frac{6}{1}$ and $\left(\frac{W}{L}\right)_P = \frac{60}{1}$. Circuit for the 4-input CMOS NOR gate is as shown below



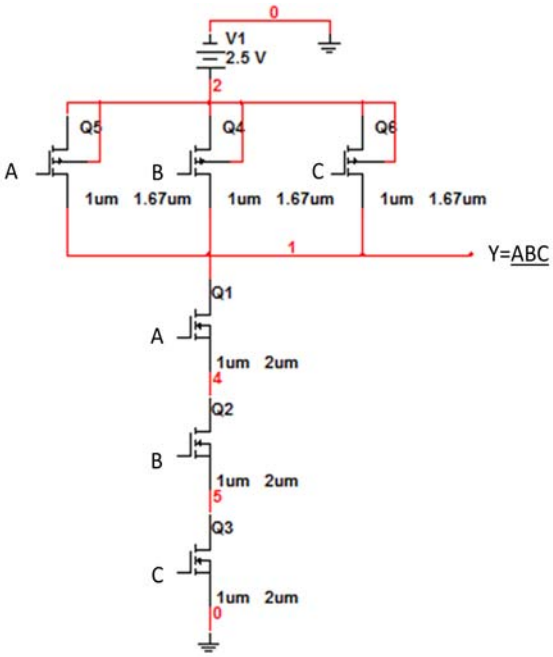
5. J&B P7.64

A current path involves 3 NMOS and 1 PMOS. Symmetrical delay requires

$$3R_{on}^{N} = R_{on}^{P}$$

$$\frac{3}{K_n'\left(\frac{W}{L}\right)_N} = \frac{1}{K_p'\left(\frac{W}{L}\right)_P}$$

$$\left(\frac{W}{L}\right)_P = \frac{1.67}{1}$$



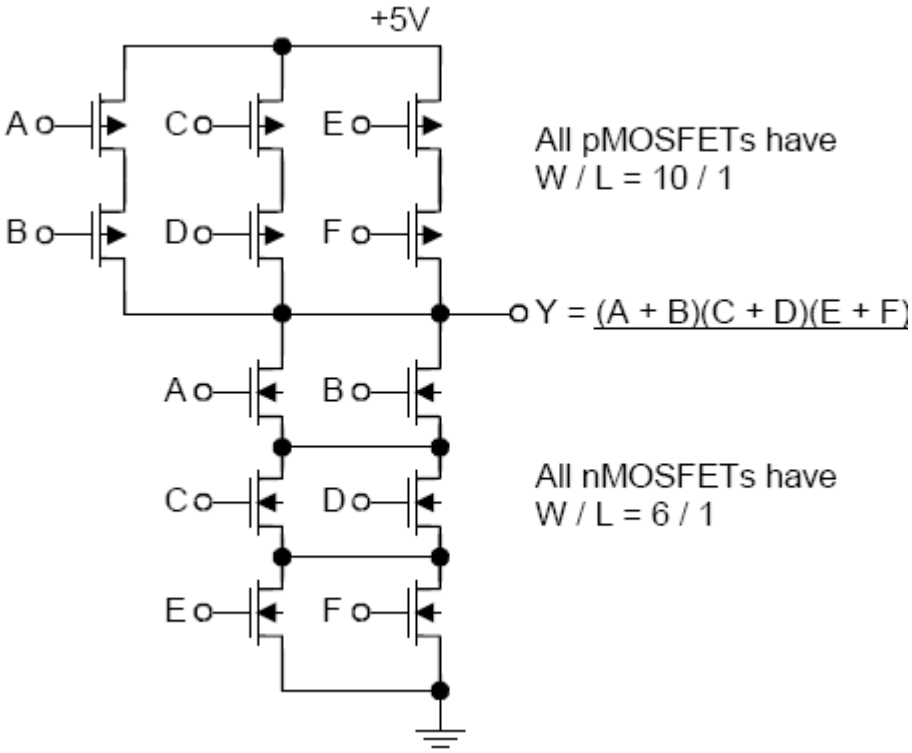
6. J&B P7.73

(a) $Y = \overline{(A+B)(C+D)(E+F)}$

(b) The complete circuit, including the PMOS network is shown below

$$\left(\frac{W}{L}\right)_N = \frac{6}{1}$$

$$\left(\frac{W}{L}\right)_P = \frac{10}{1}$$



(c)

$$\left(\frac{W}{L}\right)_{N\_eq} = \frac{1}{\left(\frac{1}{6} \div 2\right) \times 3} = \frac{4}{1}$$

(d)

$$\left(\frac{W}{L}\right)_{P\_eq} = \frac{1}{\left(\frac{1}{10} \times 2\right) \div 3} = \frac{15}{1}$$

7. J&B P7.95

The worst case involves 3 NMOS in series, with $\frac{W}{L}=\frac{2}{1}$, which is equivalent to the $R_{on}=\frac{2}{3}$, as compared to the reference inverter in which $\frac{W}{L}=\frac{2}{1}$. Thus the high to low propagation delay for this gate is three times that of the symmetrical reference inverter $\tau_{pHL}=3\tau_{pHLI}=3\times\frac{0.63C}{K_n}=4.73\,ns$.

Use numerical method introduced in lecture, we treat the whole network as a the reference inverter which includes only one NMOS and PMOS, the equivalent NMOS is with $\frac{W}{L}=\frac{2}{3}$, and the equivalent PMOS is with $\frac{W}{L}=\frac{5}{2}$.

When input suddenly is from low to high, capacitance is discharging, M_N is in on $(V_{GSN}=2.5\,V)$, and M_P is off $(V_{GSP}=0\,V)$, when $V_O=V_{DSN}>V_{GSN}-V_{TN}=V_H-V_{TN}=V_{DD}-V_{TN}=1.9\,V$, NOMS is in saturation,

$$I_C=I_{DSN}=\frac{K_n'}{2}\left(\frac{W}{L}\right)_N(V_H-V_{TNS})^2$$

when $V_O=1.9\,V$, it then is in linear,

$$I_C=I_{DN}=K_n'\left(\frac{W}{L}\right)_N\left(V_{DD}-V_{TN}-\frac{1}{2}V_O\right)V_O$$

Because the current switches operation in two regions, we consider two subsections which includes three points, calculate V_O from $V_H$to 1.9 V and 1.9 V to $V_{DD}-\frac{V_H-V_L}{2}=1.25\,V$, then $V_{DSN\_initialHL1}=2.5\,V$, $V_{DSN\_finalHL1}=1.9\,V$, $V_{DSN\_initialHL2}=1.9\,V$, $V_{DSN\_finalHL2}=1.25\,V$

$$I_{ninitHL1}=\frac{K_n'}{2}\left(\frac{W}{L}\right)_N(V_H-V_{TNS})^2=0.12\,mA$$

$$I_{ninitHL2}=I_{finalHL1}=K_n'\left(\frac{W}{L}\right)_N\left(V_{DD}-V_{TN}-\frac{1}{2}V_O\right)V_O=0.12\,mA$$

$$I_{finalHL2}=K_n'\left(\frac{W}{L}\right)_N\left(V_{DD}-V_{TN}-\frac{1}{2}V_O\right)V_O=0.106\,mA$$

$$\tau_{pHL}=\sum_n\Delta t_{nHL}=C\sum_n\frac{\Delta V_{nHL}}{I_{navgHL}}=C\sum_n\frac{\Delta V_{nHL}}{(I_{ninitHL}+I_{nfinalHL})/2}$$
$$=0.5\times10^{-12}F\times\left(\frac{0.6\,V}{0.12\,mA}+\frac{0.65\,V}{0.113\,mA}\right)=5.38\text{ ns}$$

Consider three subsections which includes 4 points, calculate V_O from $V_H$to 1.9 V, 1.9 V to 1.4 $V$and 1.4 V to 1.25 V then $V_{DSN\_initialHL1}=2.5\,V$, $V_{DSN\_finalHL1}=1.9\,V$, $V_{DSN\_initialHL2}=1.9\,V$, $V_{DSN\_finalHL2}=1.4\,V$, $V_{DSN\_initialHL2}=1.4\,V$, $V_{DSN\_finalHL2}=1.25\,V$, then

$$I_{ninitHL1} = 0.12\ mA$$

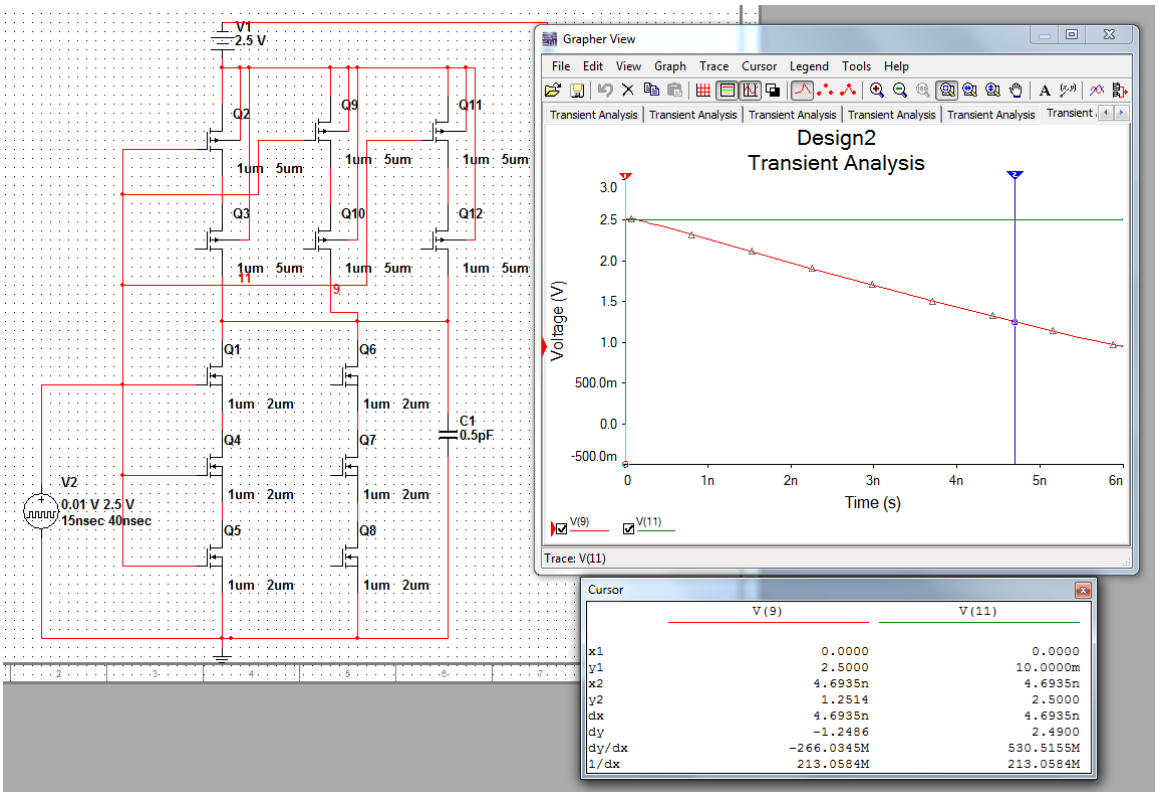
$$I_{ninitHL2} = I_{finalHL1} = 0.12\ mA$$

$$I_{ninitHL3} = I_{finalHL2} = 0.112\ mA$$

$$I_{finalHL3} = 0.106\ mA$$

$$\tau_{pHL} = 0.5 \times 10^{-12} F \times \left(\frac{0.6\ V}{0.12\ mA} + \frac{0.5\ V}{0.116\ mA} + \frac{0.15\ V}{0.109\ mA}\right) = 5.34\ \text{ns}$$

Compared with Multisim result



$$\tau_{pHL} = 4.7\ ns$$

8. J&B P7.116

From the Fig. 7.36 of the text book, the maximum occurs when NMOS transistor is cutoff,

$$R_{onn} = \infty$$

PMOS is in triode ($V_{DSP} \approx 0$), and the combined resistance becomes R_{onp} which is decreasing in value thereafter,

$$R_{EQ} = R_{onp}$$

The resistance of PMOS

$$R_{onp} = \frac{V_{DSP}}{I_{DSP}} = \frac{V_{DSP}}{K_p{}'\left(\frac{W}{L}\right)_P \left(V_{GSP} - V_{TP} - \frac{1}{2}V_{DSP}\right) V_{DSP}} \approx \frac{V_{DSP}}{K_p{}'\left(\frac{W}{L}\right)_P (V_{GSP} - V_{TP}) V_{DSP}}$$
$$= \frac{1}{K_p{}'\left(\frac{W}{L}\right)_P (V_{GSP} - V_{TP})} \leq 250\ \Omega$$

When $\left(\frac{W}{L}\right)_P$ are minimum, the R_{EQ} is maximum, then

$$\frac{1}{K_p{}'\left(\frac{W}{L}\right)_{P\_min} (V_{GSP} - V_{TP})} = 250\ \Omega \quad \blacksquare$$

$$V_{TP} = V_{TOP} - \gamma_P\left(\sqrt{V_{SBP} + 2\varphi_{FP}} - \sqrt{2\varphi_{FP}}\right)$$

In order to obtain the source voltage when NMOS is cutoff, we let

$$V_{GSN} = V_{TN}$$

or

$$2.5\ V - V_S = V_{TON} + \gamma_N\left(\sqrt{V_S + 2\varphi_{FN}} - \sqrt{2\varphi_{FN}}\right)$$

Use iterative algorithm or mathematic software to solve for above equation, we get

$$V_S = 1.426\ V$$

Plug this back to equation ■ with appropriate V_{TP}, we get

$$\left(\frac{W}{L}\right)_{Pmin} = \frac{240}{1}$$

Similar approach can be used to solve the $\left(\frac{W}{L}\right)_{Nmin}$ if the maximum happens when PMOS is cutoff and NMOS is in triode. When PMOS transistor is cutoff,

$$R_{onp} = \infty$$

NMOS is in triode ($V_{DSN} \approx 0$), and the combined resistance becomes R_{onn} which is decreasing in value thereafter,

$$R_{EQ} = R_{onn}$$

The resistance of NMOS

$$R_{onn} = \frac{V_{DSN}}{I_{DSN}} = \approx \frac{1}{K_n{}' \left(\frac{W}{L}\right)_N (V_{GSN} - V_{TN})} \leq 250\ \Omega$$

Then

$$\frac{1}{K_n{}' \left(\frac{W}{L}\right)_{N\_min} (V_{GSN} - V_{TN})} = 250\ \Omega \quad \blacksquare\blacksquare$$

$$V_{TN} = V_{TON} + \gamma_N \left(\sqrt{V_S + 2\varphi_{FN}} - \sqrt{2\varphi_{FN}}\right)$$

In order to obtain the source voltage when PMOS is cutoff, we let

$$V_{GSP} = V_{TP}$$

$$-V_S = V_{TOP} - \gamma_P \left(\sqrt{V_{SBP} + 2\varphi_{FP}} - \sqrt{2\varphi_{FP}}\right)$$

Use iterative algorithm or mathematic software to solve above equation, we get

$$V_S = 1.07433\ V$$

Plug this back to equation ■■ with appropriate V_{TN}, we get

$$\left(\frac{W}{L}\right)_{Nmin} = \frac{96.2}{1}$$