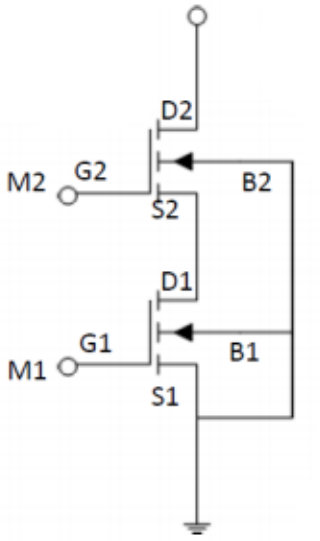
Homework 9 Solutions

1. For the circuit as shown below, the two gates are connected together. We consider that both the NMOSs are working in the triode region. For the transistor, $V_{SB1} = 0$, so $V_{TN1} = V_{TNO}$; for the upper transistor, $V_{SB2} = V_{DS1}$, so $V_{TN2} = V_{TNO} + \alpha V_{DS1}$. Denote the voltage on the intermediate point (D1,S2) as V_O, then

$$\left(V_{GG} - V_{TNO} - \frac{(1+\alpha)V_O}{2}\right)V_O = \left((V_{GG} - V_O) - (V_{TNO} + \alpha V_O) - \frac{(1+\alpha)(V_{DD} - V_O)}{2}\right)(V_{DD} - V_O)$$



Solving this equation (you can use mathematica or maple or matlab) gives:

$$V_O = \frac{\left(2V_{GG} - 2V_{TNO} + \sqrt{\blacksquare}\right)}{2(1+\alpha)}$$

$$\blacksquare = 2\left(\alpha^2 {V_{DD}}^2 + 2\alpha {V_{DD}}^2 - 2\alpha V_{GG}V_{DD} + 2\alpha V_{DD}V_{TNO} + {V_{DD}}^2 - 2V_{GG}V_{DD} + 2V_{DD}V_{TNO} + 2{V_{GG}}^2 - 4V_{GG}V_{TNO} + 2{V_{TNO}}^2\right)$$

This expression can be plugged back into the current equation giving:

$$I_{D1} = K_n'\left(\frac{W}{L}\right)_1\left(V_{GG} - V_{TNO} - \frac{(1+\alpha)V_O}{2}\right)V_O = \frac{1}{2}K_n'\left(\frac{W}{L}\right)_1\left(V_{GG} - V_{TNO} - \frac{(1+\alpha)V_{DD}}{2}\right)V_{DD}$$

Which is exactly the current for a device with twice the length of the original MOSFETs (L⇒2L).

Using numbers, let $\alpha = 0.2$, and assume the first pair has $\left(\frac{W}{L}\right)_1 = \frac{1}{1}$, $V_{GG} = 3\,V$, $V_{DD} = 2\,V$, $V_{TNO} = 0.5\,V$ as suggested on GoPost.

The drain current for each NMOS in one pair should be same. For the lower transistor, $V_{SB1} = 0$, so $V_{TN1} = V_{TNO} = 0.5\,V$; for the upper transistor, $V_{SB2} = V_{DS1}$, so $V_{TN2} = V_{TNO} + \alpha V_{DS1} = 0.5\,V + \alpha V_{DS1}$. We assume both devices are in triode, denoting the voltage on the intermediate point as V_O, then

$$\left(V_{GG} - V_{TNO} - \frac{(1+\alpha)V_O}{2}\right)V_O = \left(V_{GG} - V_O - V_{TNO} - \alpha V_O - \frac{(1+\alpha)(V_{DD} - V_O)}{2}\right)(V_{DD} - V_O)$$

Solving the equation, we get

$$V_O = 0.609\,V$$

Check our assumption, for lower NMOS, $V_{GS1} > V_{TN1}$, $V_{GS1} - V_{TN1} = 2.5\,V > (1+\alpha)V_{DS1}$; for upper NMOS, $V_{GD2} = 1\,V > V_{TNO} + \alpha V_{DD} = 0.9\,V$, then assumption is correct.

$$I_{D1} = K_n'\left(\frac{W}{L}\right)_1\left(V_{GG} - V_{TNO} - \frac{(1+\alpha)V_O}{2}\right)V_O = 130\,\mu A$$

For another NMOS with $\left(\frac{W}{L}\right) = \frac{1}{2}$,

$$I_{D2} = K_n'\left(\frac{1}{2}\right)\left(V_{GG} - V_{TNO} - \frac{(1+\alpha)V_{DD}}{2}\right)V_{DD} = 130\,\mu A$$

Then currents are equal as found above symbolically.

Note that if we use the body effect for the upper transistor, but ignore the distributed body effect (no α in current equations). The currents are not equal (try it yourself).

2. As $V_{GS} - V_{TN} = -0.1\,V$, nMOS works in sub-threshold region.

Channel mobility of a 10^{17} cm^{-3} doped bulk silicon is $\mu_n = \mu_{nbulk}/2 = 400$ cm^2/Vs

$$C_{ox}'' = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}} = 7.1\text{x}10^{-7}\ \text{F/cm}^2$$

$$x_d = \sqrt{\frac{2\varepsilon_{si}\varepsilon_0}{qN_a}2\frac{kT}{q}\ln\frac{N_a}{n_i}} = 103\ \text{nm}$$

$$\alpha = \frac{C_d^{"}}{C_{ox}^{"}} = \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} x_d} = 0.146$$

$$\Delta V = (1+\alpha)\frac{kT}{q} = 0.0292 \text{ V}$$

$$i_{Dsub} = \left(\frac{Q_I^{'}}{L}\right)\mu_n \frac{kT}{q}\left(1 - e^{-qv_{DS}/kT}\right) = \frac{W}{L} C_{ox}^{"} \Delta V \exp\left(\frac{V_{GS} - V_T - \Delta V}{\Delta V}\right)\mu_n \frac{kT}{q}\left(1 - e^{-qv_{DS}/kT}\right)$$

$$= 2.58\text{x}10^{-9}\left(1 - e^{-qv_{DS}/kT}\right)$$

Assume $V_{DS} >> kT/q$, $i_{Dsub} \approx 2.58 \times 10^{-9} A$, nearly independent of V_{DS}

$$C\frac{V_{initial}}{2} = \Delta Q = i_{Dsub} t$$

Then, the time required to drop voltage to 50% is

$$t = \frac{CV_{initial}}{2i_{Dsub}} = 1.94 \times 10^{-4} V_{\text{initial}} \text{ s}$$

3. J&B P7.55

$$PDP = P_{av}\tau_p$$

$$P_{av} = CV_{DD}^2 f$$

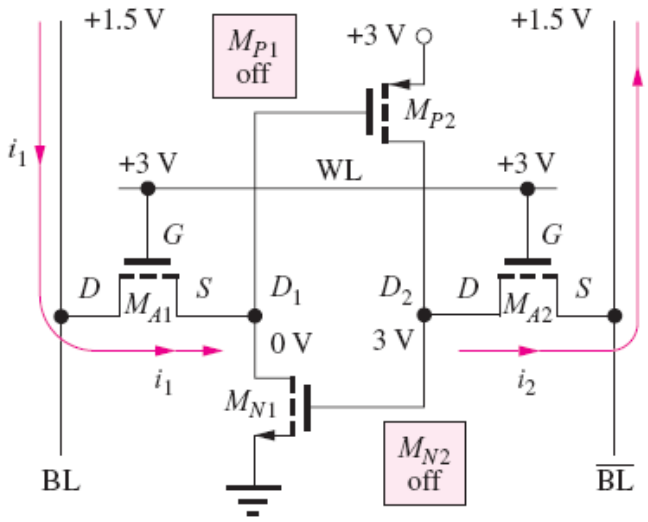
$$f = 1/T$$

T is proportion a3nal to τ_p, τ_p is proportional to C, so when capacitance is scaling with factor of α, $PDP = \frac{CV_{DD}^2}{T} * \tau_p \propto \alpha^3$

4. J&B P7.83

In order to be twice faster compared with the reference inverter with a load of capacitance of 2C, $\left(\frac{W}{L}\right)_{N\_equ} = \frac{8}{1}$, $\left(\frac{W}{L}\right)_{P\_equ} = \frac{20}{1}$. The worst path contains 3 NMOS and 2 PMOS, hence $\left(\frac{W}{L}\right)_N = \frac{24}{1}$, $\left(\frac{W}{L}\right)_P = \frac{40}{1}$

5. J&B P8.6



Because the bitlines are fixed at 1.5 V, as current increases through M_{A1} and M_{A2}, the voltage on data node D1 tends to rise, but have to be below 0.7 V, and the voltage at D2 tends to fall, but have to be above 2.3 V. Then in the final steady-state condition, M_{A1} will be on in the triode region because for M_{A1}, $V_{DS} = 0.8\,V < V_{GS} - V_{TN} = 1.6\,V$ and M_{A2} will be on in the saturation region, because $V_{DS} = 0.8\,V = V_{GS} - V_{TN} = 0.8\,V$. M_{N1} is in triode and M_{P2} is in also in triode. Then

$$\left(\frac{W}{L}\right)_{A1\_max}\left(1.6-\frac{1}{2}\times 0.8\right)0.8 = \left(\frac{W}{L}\right)_{N1}\left(1.6-\frac{1}{2}\times 0.7\right)0.7$$

$$K_n'\left(\frac{W}{L}\right)_{A2\_max}\left(0.8-\frac{1}{2}\times 0.8\right)0.8 = K_p'\left(\frac{W}{L}\right)_{P2}\left(1.6-\frac{1}{2}\times 0.7\right)0.7$$

$$\left(\frac{W}{L}\right)_{A1\_max} = \frac{0.912}{1}$$

$$\left(\frac{W}{L}\right)_{A2\_max} = \frac{1.094}{1}$$