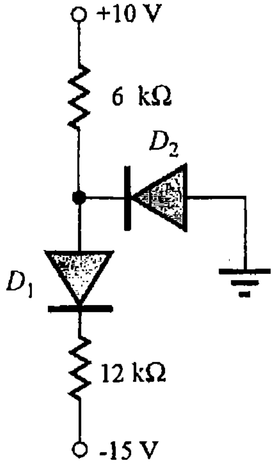
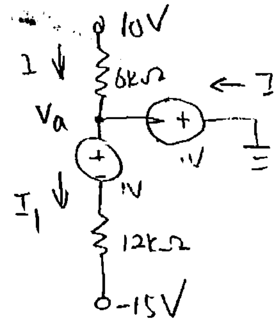
1. (12 pts) Find the Q-point for the diodes D_1 and D_2 shown in the figure below using the constant voltage drop (CVD) model with $V_{on} = 1$ V. Give answers for **BOTH** diodes.



Assume both diodes are ON.



$V_a = -V_{on} = -1V$

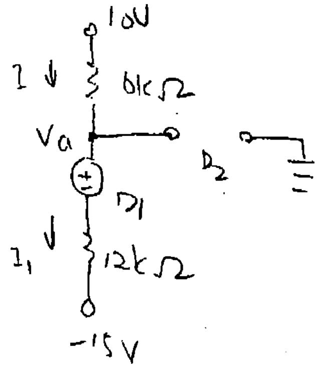
$I = \frac{10V - (-1)V}{6k\Omega} = 1.83mA$

$I_1 = \frac{(-1-1+15)V}{12k\Omega} = 1.08mA$

$I_2 = I_1 - I = -0.75mA < 0$

Inconsistent with D_2 ON!

Thus D_1 ON, D_2 OFF



$I = I_1 = \frac{10V - (-15V) - 1V}{(6+12)k\Omega} = 1.33mA$

$V_a = 10V - IR = 10 - 1.33mA \cdot 6k\Omega = 2V$

$V_{D2} = -V_a = -2V$

Q-pt for D_1 (1.33mA, 1V)

Q-pt for D_2 (0A, -2V)

Check $I_{D1} > 0$, $V_{D1} = V_{on}$, consistent with D_1 ON

$I_{D2} = 0$, $V_{D2} = -2V < V_{on}$, consistent with D_2 OFF

3. (25 points) In the following circuit, use the constant voltage diode model with a threshold (turn-on) voltage of 0.8 V. Assume the diodes **D_1 and D_2 are on** and the diode **D_3 is off.**

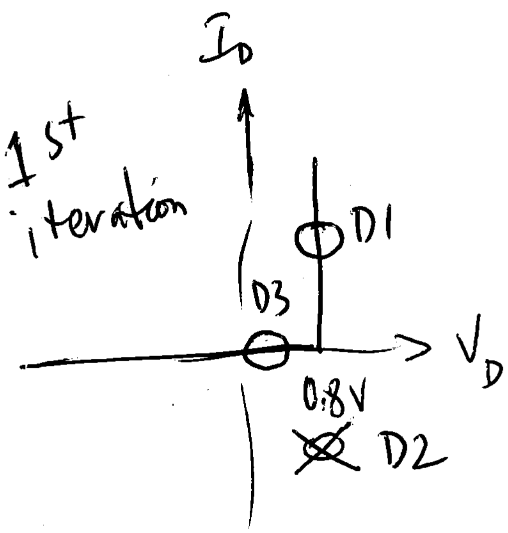
a) (5 pt) Calculate the voltage across each diode.

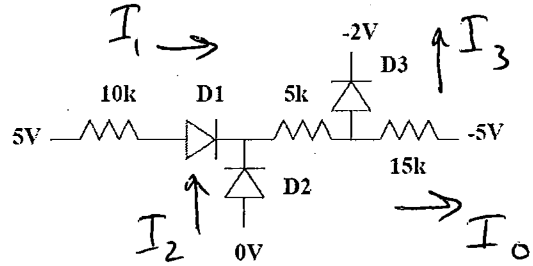
b) (5 pt) Calculate the current through each diode.

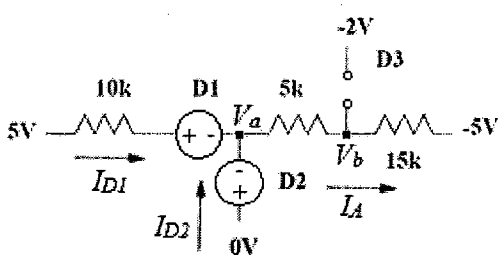
c) (5 pt) Check your assumptions for D_1 -- are they correct? Why or why not?

d) (5 pt) Check your assumptions for D_2 -- are they correct? Why or why not?

e) (5 pt) Check your assumptions for D_3 -- are they correct? Why or why not?







According to the assumption: $V_{D1} = 0.8$ V, $V_{D2} = 0.8$ V, $I_{D3} = 0$.

$V_a = -0.8$ V, $I_{D1} = \frac{5\text{ V} - 0.8\text{ V} - (-0.8\text{ V})}{10\text{ k}\Omega} = 0.50$ mA.

$$I_A = \frac{0\text{ V} - 0.8\text{ V} - (-5\text{ V})}{15\text{ k}\Omega + 5\text{ k}\Omega} = 0.21\text{ mA}.$$

$I_{D2} = I_A - I_{D1} = -0.29$ mA

$V_b = V_a - 5\text{ k}\Omega \cdot 0.21\text{ mA} = -1.85$ V

$V_{D3} = V_b - (-2\text{ V}) = 0.15$ V

D_1: $V_{D1} = 0.8$ V, $I_{D1} = 0.50$ mA. $I_{D1} > 0$, assumption for D_1 being on is correct.

D_2: $V_{D2} = 0.8$ V, $I_{D2} = -0.29$ mA. $I_{D2} < 0$, assumption for D_2 being on is NOT correct.

D_3: $I_{D3} = 0$, $V_{D3} = 0.15\text{ V} < 0.8$ V. $V_{D3} < V_{on}$, assumption for D_3 being off is correct. if D_2 is ON as assumed.

With D2 off, D3 on, D1 on:

$$V_b = -5V + I_o * 15k\Omega \quad , \quad I_o = \frac{5V - V_{on} - (-5V)}{10k + 5k + 15k} = \frac{9.2V}{30k\Omega}$$

$$= -5V + \frac{9.2V}{30k\Omega} 15k\Omega \qquad = 0.307\ mA$$

$$= -5V + 4.6V = -0.4V$$

$$V_{D3} = -0.4 - (-2V) = 1.6V > V_{on} \Rightarrow \text{D3 not OFF}$$

With D2 off and D3 on (and D1 still on)

$$V_b = -2V + V_{on} = -1.2V$$

$$I_1 = \frac{5V - V_{on} - V_b}{15k\Omega} = \frac{5.4V}{15k\Omega} = 0.36mA$$

$$V_a = 5V - V_{on} - I_1 (10k\Omega)$$

$$= 5V - 0.8V - \frac{5.4V}{15k\Omega} 10k\Omega$$

$$= 5V - 0.8V - 3.6V = 0.6V$$

$$V_{D2} = 0 - 0.6V = -0.6V \Rightarrow \text{OFF}$$

$$I_3 = I_1 - \frac{V_b - (-5V)}{15k\Omega} = 0.36mA - \frac{3.8V}{15k\Omega} = 0.36mA - 0.253mA$$

$$= 0.107\ mA > 0$$

D1, on $\quad V_{D1} = 0.8V \quad I_1 = 0.36mA$

D2, off $\quad V_{D2} = -0.6V \quad I_2 = 0$

D3, on $\quad V_{D3} = 0.8V \quad I_3 = 0.107mA$

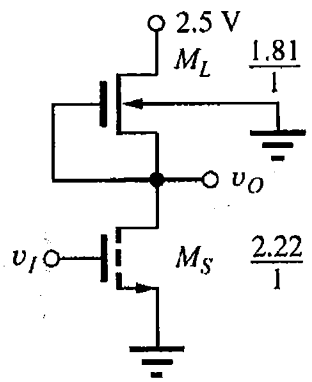
(16 pts) You are asked to design an NMOS logic gate that implements

$$Y = \overline{A(B + CD) + E}$$

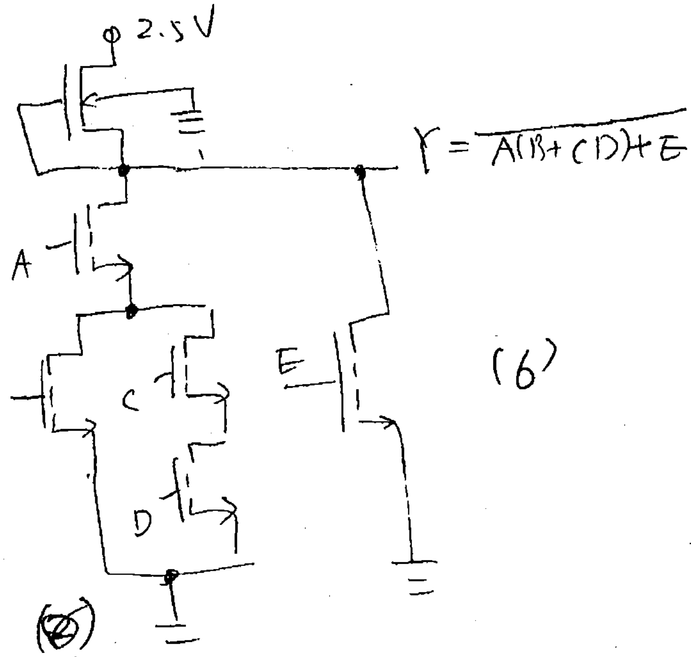
based on the reference inverter shown below.

(a) (6 pts) Draw the circuit diagram.

(b) (10 pts) Find the W/L ratios of all transistors in the circuit such that the propagation delay (τ_P) is 1/2 the delay of the reference inverter below. (Hint: $\tau_P \propto R_{on}C$)



(a)



(b)

$\tau \sim R_{on}C \propto \left(\frac{W}{L}\right)^{-1}$

$\tau \to \frac{1}{2}\tau \Rightarrow \left(\frac{W}{L}\right) \to 2\left(\frac{W}{L}\right)$ (2)

(b) M_L should have $\left(\frac{W}{L}\right)$ doubled, $\left(\frac{W}{L}\right)_L = \frac{3.62}{1}$

Let on-resistance of M_S to be R_{on}^S.

Pick worse case path ACD.

$R_A + R_C + R_D = \frac{1}{2}R_{on}^S$ (½ delay)

(i) $R_A = R_C = R_D = \frac{1}{6}R_{on}^S$, $R_B = \frac{1}{3}R_{on}^S$. $R_E = \frac{1}{2}R_{on}^S$.

$\left(\frac{W}{L}\right)_{A,C,D} = 6\left(\frac{2.22}{1}\right) = \frac{13.32}{1}$, $\left(\frac{W}{L}\right)_B = 3 \cdot \frac{2.22}{1} = \frac{6.66}{1}$

$\left(\frac{W}{L}\right)_E = \frac{4.44}{1}$ 2.

(ii) $R_A = \frac{1}{4}R_{on}^S$, $R_C = R_D = \frac{1}{8}R_{on}^S$, $R_B = \frac{1}{4}R_{on}^S$, $R_E = \frac{1}{2}R_{on}^S$

$\left(\frac{W}{L}\right)_{A,B} = 4\left(\frac{2.22}{1}\right) = \frac{8.88}{1}$, $\left(\frac{W}{L}\right)_{C,D} = 8 \cdot \frac{2.22}{1} = \frac{17.76}{1}$.

$\left(\frac{W}{L}\right)_E = \frac{4.44}{1}$