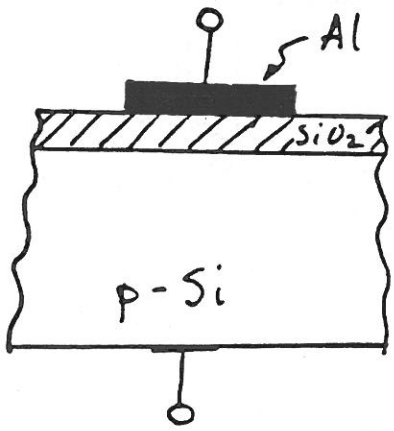
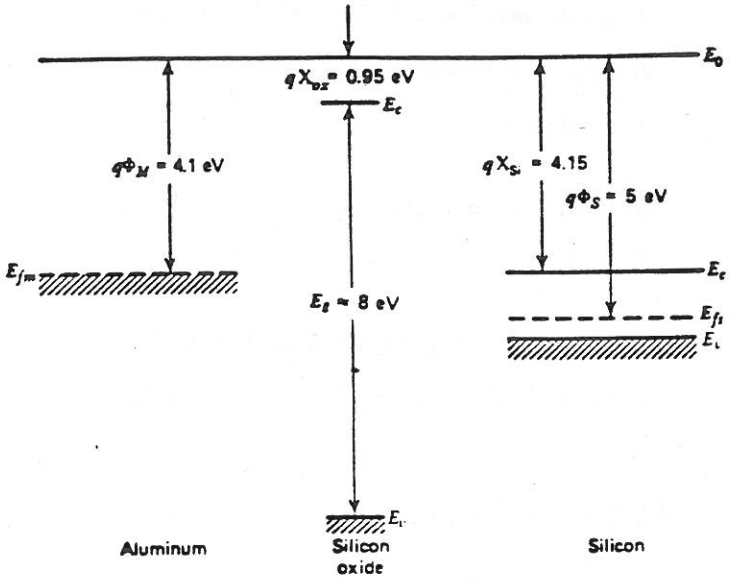
MOS Capacitors

We need to describe the physics of one additional two terminal device before we proceed on to three terminal structures.





MOS Structure
p- substrate
Al gate

Note:

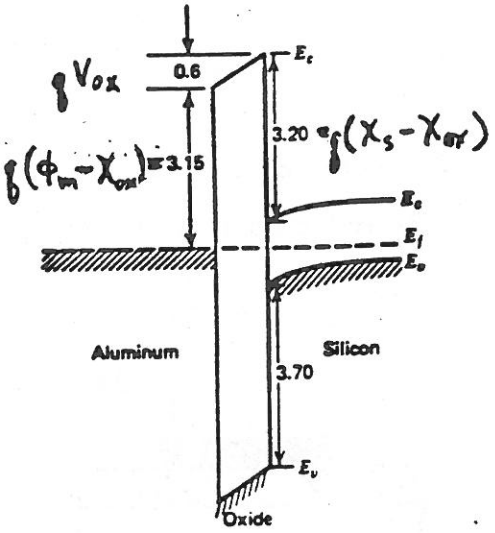
1. Bringing 3 materials into contact $\Rightarrow E_f$ = constant, just as in PN junctions.
2. Currents through SiO_2 are very small, therefore must wait a long time for equilibrium to be established or provide alternative path.
3. Holes at higher average energy in P silicon than in aluminum (energy of holes greater in negative direction)

   holes $\rightarrow$ metal on contact

   electrons $\rightarrow$ silicon on contact

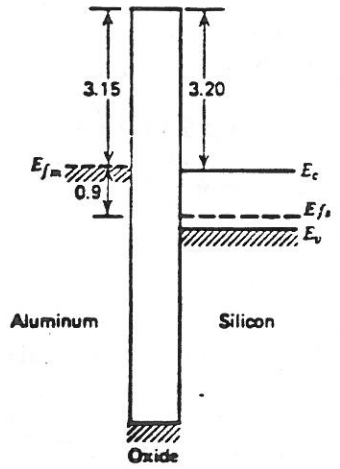
   Therefore, bands will bend down in silicon at surface ($\phi_m < \phi_s$).

No Applied Voltage on Gate



- Abrupt transition in E_c and E_v levels at material interfaces.
- Potential drop across SiO_2 can be supported because no current flows through SiO_2. Typical value is 0.6 eV and depends on solution of Poisson's equation across oxide and silicon.
- Substantial barriers exist to current flow $S \rightarrow M$ and $M \rightarrow S$.
- Depletion region exists near the surface because E_f is further from E_v than in bulk.

Applied Bias



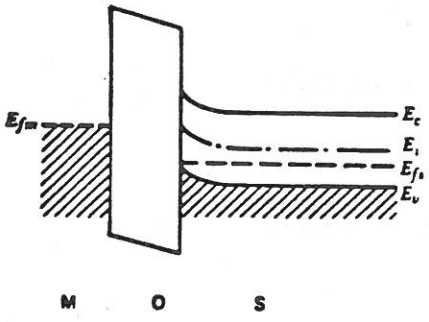
Negative voltage on gate:

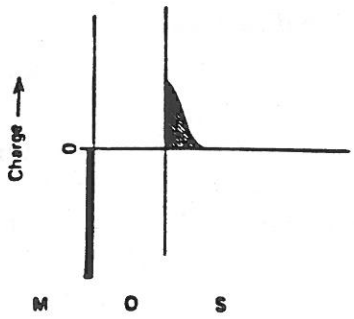
- E_f is still constant in silicon since SiO_2 prevents any current flow.
- E_f is closer to E_v at the surface, therefore more holes near surface.

  $\Rightarrow$ FLAT BAND and then ACCUMULATION

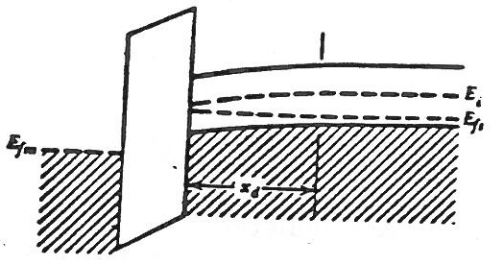
  $$V_{FB} = \phi_m - \phi_s = \Phi_{MS}$$

- **Flat band is not equilibrium.**



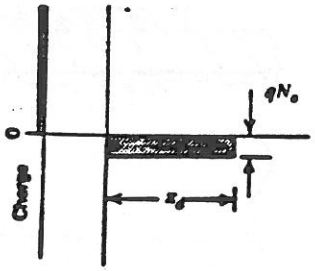


Positive Voltage on gate:

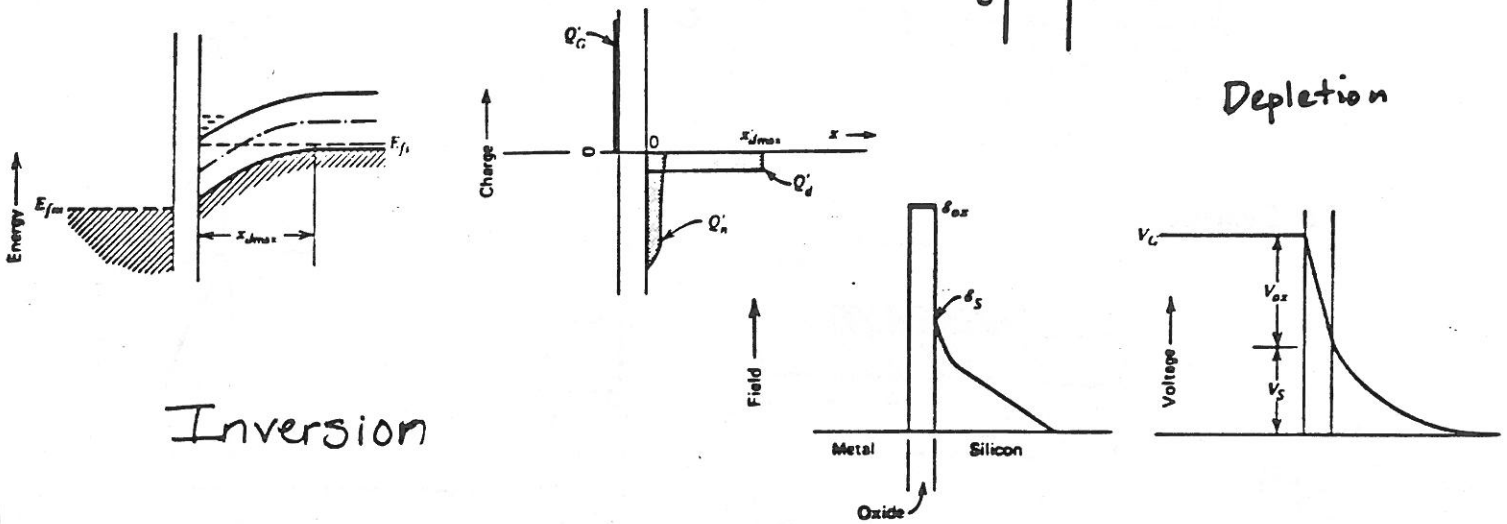


- E_f is still constant in silicon ($I = 0$).
- E_f moves closer to E_c and further from E_v at the surface. Therefore concentration of electrons increases and concentration of holes decreases.

  $\Rightarrow$ DEPLETION and then INVERSION



Depletion



Inversion

Carrier Concentrations in Thermal Equilibrium

At any point in the silicon,

$$p = n_i \exp\left(-\frac{q\phi(x)}{kT}\right) \tag{1}$$

$$n = n_i \exp\left(\frac{q\phi(x)}{kT}\right) \tag{2}$$

where $\phi(x) = \Big(E_f - E_i(x)\Big)/q$.

In terms of the surface potential ϕ_s and the bulk potential ϕ_p (negative),

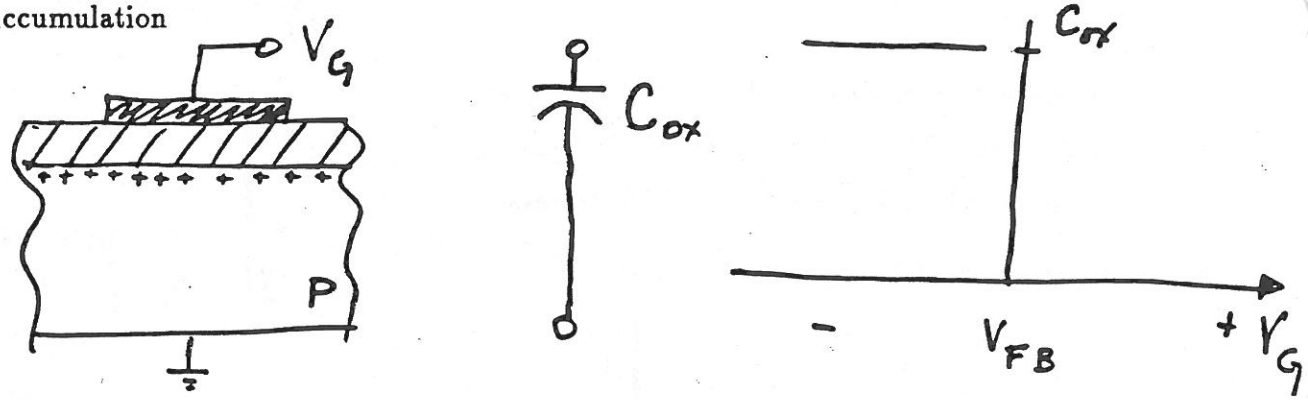
$$p_s = N_a \exp\left[\frac{q(\phi_p - \phi_s)}{kT}\right] \tag{3}$$

$$n_s = \frac{{n_i}^2}{N_a} \exp\left[\frac{q(\phi_s - \phi_p)}{kT}\right] \tag{4}$$

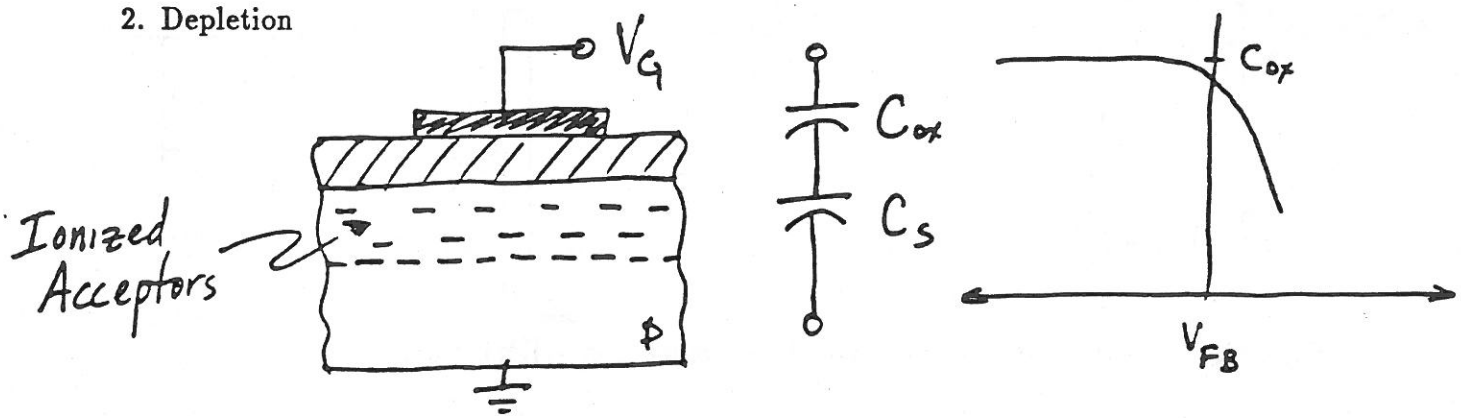
therefore, since we know ϕ_p from the bulk doping, if we know ϕ_s for a given applied V_G, then we can calculate the electron and hole surface concentrations.

Capacitance-Voltage Characteristics

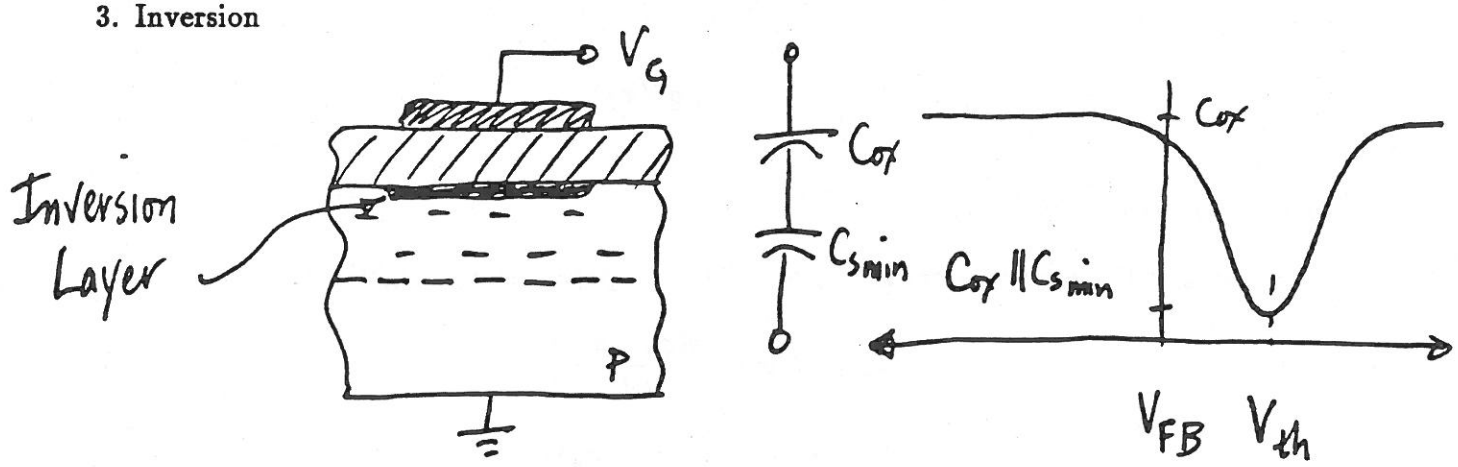
1. Accumulation



2. Depletion



3. Inversion



A simple MOS capacitor illustrates the three main regions of device operation.

$$C'_{ox} = \frac{K_{ox}\epsilon_0}{x_{ox}} = \text{oxide capacitance / unit area} \tag{5}$$

During depletion,

$$\frac{C'}{C'_{ox}} = \frac{1}{1 + C'_{ox}\frac{x_d}{\epsilon_s}} = \frac{1}{\sqrt{1 + \frac{2K_{ox}{}^2\epsilon_0}{qN_aK_s{x_{ox}}^2}(V_G - V_{FB})}} \tag{6}$$

Inversion occurs when

$$\phi_s = -\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i}$$

where ϕ_F is the bulk electron potential ϕ_p or ϕ_n (P:−, N:+).

At this potential, for a p-type substrate,

$$x_{d\max} = \sqrt{\frac{2K_s\epsilon_0}{qN_a}|2\phi_F|} \tag{7}$$

Note that the maximum change in ϕ_s is $\approx -2\phi_F$ since heavy inversion clamps ϕ_s and any further change in gate voltage causes a very large change in the inversion charge near the interface.

$$C'_{\min} = \frac{1}{1/C'_{ox} + 1/C'_{s\min}} \tag{8}$$

where

$$C'_{s\min} = \frac{1}{\sqrt{\frac{4kT}{q^2\epsilon_s N_a}\ln\frac{N_a}{n_i}}} \tag{9}$$

For a n-type substrate, N_d must be substituted for N_a.

The voltage between the gate and the bulk of the semiconductor is the sum of the flatband voltage, the voltage drop across the semiconductor and the voltage drop across the oxide. The gate voltage at which $\phi_s = -\phi_F$ is called the threshold voltage V_{th}, or the edge of strong inversion. At the edge of strong inversion,

$$V_s = -2\phi_F \tag{10}$$

$$V_{ox} = -\frac{Q'_B}{C'_{ox}} = \frac{\sqrt{2q\epsilon_s N_a|2\phi_F|}}{C'_{ox}} \tag{11}$$

since in p-type material the ionized acceptors in the depletion region are negatively charged.

Therefore,

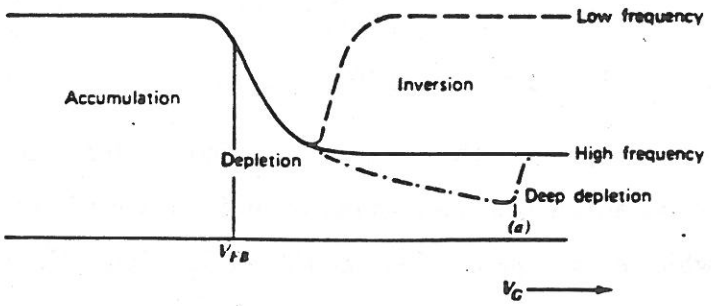
$$V_{th} = \Phi_{MS} - 2\phi_F - \frac{Q'_B}{C'_{ox}} \tag{12}$$

$$Q'_B = -qN_a x_{d\max} \text{ or } qN_d x_{d\max}$$

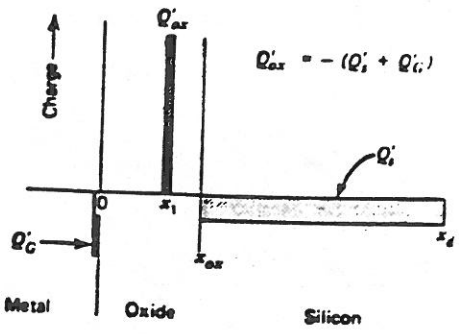
Actually, the C-V characteristics of a MOS capacitor in inversion depend on the both the sweep rate and signal frequency. The inversion layer is slow to form since the only source of electrons is thermal generation.

$$\text{time to form inversion layer} \approx \left(\frac{2N_a\tau_0}{n_i}\right) \sim 0.2\,\text{sec}$$

- Slow sweep rate, low frequency. The inversion layer has time to form so charge is added to inversion layer and $C' \approx C'_{ox}$
- Slow sweep rate, high frequency. The inversion layer has time to form but cannot respond to high frequency signal which modulates depletion region width. $C' \approx C'_{ox} \parallel C'_{s\min}$.
- Fast sweep rate. The inversion layer does not have time to form so substrate is depleted beyond $x_{d\max}$ and $C' < C'_{ox} \parallel C'_{s\min}$. Eventually the depletion region gets wide enough that the electron generation rate is large enough to form inversion layer.



Non-Ideal Effects in the MOS Structure

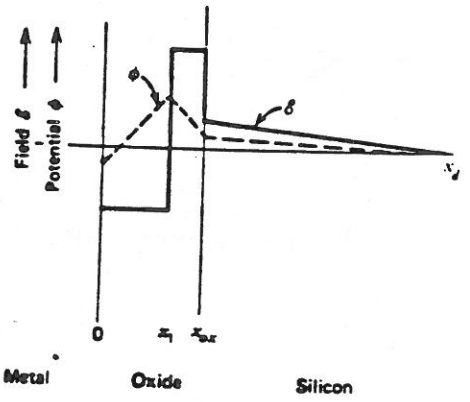


Actual C-V curves are shifted laterally from the theoretical curve due to:

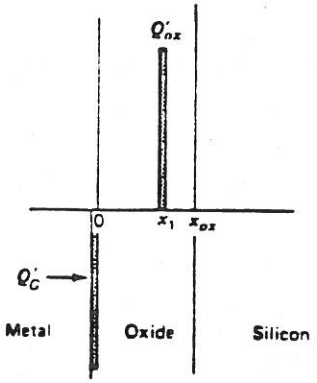
1. Work function differences between metal and semiconductor $\phi_m - \phi_s = \Phi_{MS}$. Can also use polysilicon gate in which case $\Phi_{MS} = \phi_{s\,\text{gate}} - \phi_{s\,\text{sub}}$.

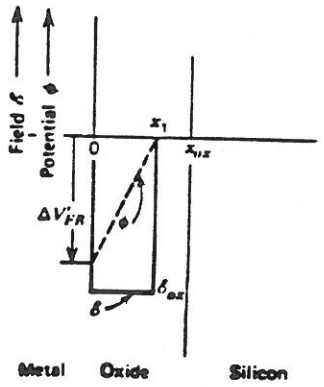
2. Q'_{ss}: Charge at the Si-SiO_2 interface. Usually positive. Due to broken bonds at interface and excess silicon in oxide.

3. Q'_{ox}: Charge within the oxide. Usually positive. Trapped holes due to radiation or avalanche breakdown and mobile alkali metal ions.



$$V_{th} = \underbrace{\Phi_{MS} - \frac{Q'_{ss}}{C'_{ox}} - \frac{1}{C'_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x)\, dx}_{\text{Flatband Voltage}} - 2\phi_F - \frac{\sqrt{2q\epsilon_s N_a |2\phi_F|}}{C'_{ox}} \qquad (13)$$





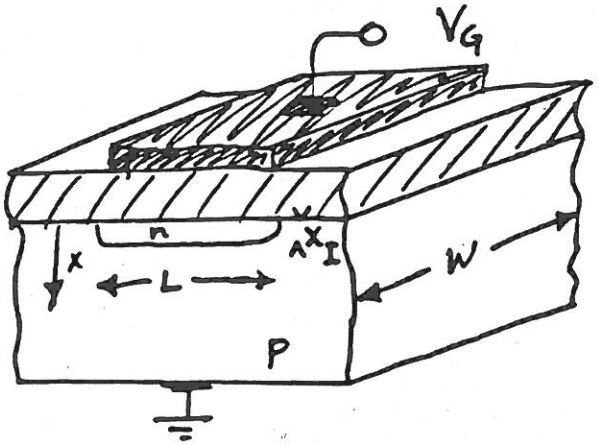
Note: If a C-V curve is measured

1. x_{ox} can be calculated from C'_{ox}.

2. N_a can be calculated from C'_{min}.

3. Weighted combination of Q'_{ss} and $Q'_{ox} = \int_0^{x_{ox}} \rho(x)\, dx$ can be calculated from shift. Charges which are farther from the gate have a greater effect on V_{th}.

Inversion Layer Conductance



Suppose we apply a potential large enough to cause inversion i.e. $V_G > V_{th}$.

The conductance (1/R) of the inversion layer is given by

$$g_I = \frac{1}{R_I} = \frac{W}{L}\int_0^{x_I} q\mu_n n_I(x)\,dx \tag{14}$$

where $n_I(x)$ = electron density in inversion layer

x_I = depth of inversion layer

μ_n' = electron mobility in inversion layer ($\sim$ 1/2 bulk mobility)

But,

$$\int_0^{x_I} q n_I(x)\,dx = -Q_I' = \text{inversion layer charge / unit area} \tag{15}$$

Therefore,

$$g_I = -\frac{W}{L}\mu_n' Q_I' \qquad \text{(electrons are } -\text{)} \tag{16}$$

Using our definition of V_{th}, we have

$$\begin{aligned} V_{th} - V_{FB} &= -2\phi_F + \frac{\sqrt{2q\epsilon_s N_a |2\phi_F|}}{C_{ox}'} \\ &= -2\phi_F - \frac{Q_B'}{C_{ox}'} \end{aligned} \tag{17}$$

where Q_B' is the charge in the surface depletion layer when $x_d = x_{d\max}$, i.e. under strong inversion.

The total voltage across the structure is

$$V_G - V_{FB} = \Delta V_{ox} - 2\phi_F \tag{18}$$

where, ΔV_{ox} is the change in voltage drop across the oxide due to the charge in the semiconductor (difference from flatband).

Using Gauss' Law,

$$Q'_s = -K_s\epsilon_0\mathcal{E}_s = -K_{ox}\epsilon_0\mathcal{E}_{ox} = -K_{ox}\epsilon_0\frac{V_{ox}}{x_{ox}} = -C'_{ox}V_{ox}$$

Therefore, due to Q'_s which is the total charge in the silicon,

$$\Delta V_{ox} = -\frac{Q'_s}{C'_{ox}} = \frac{\Delta Q'_g}{C'_{ox}} \tag{19}$$

Therefore, from (18),

$$V_G - V_{FB} = -\frac{Q'_s}{C'_{ox}} - 2\phi_F \tag{20}$$

Now, under strong inversion,

$$\begin{aligned} Q'_s &= Q'_I + Q'_B \\ &= Q'_I - qN_a x_{d\max} \end{aligned} \tag{21}$$

Substituting into (20)

$$V_G = V_{FB} - \left(\frac{Q'_I + Q'_B}{C'_{ox}}\right) - 2\phi_F \tag{22}$$

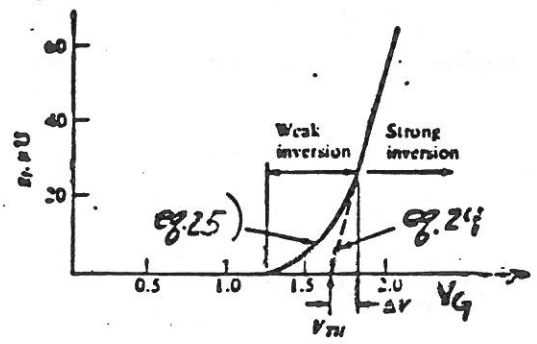
$$V_G - V_{th} = -\frac{Q'_I}{C'_{ox}} \tag{23}$$

$$g_I = \frac{W}{L}\mu'_n C'_{ox}(V_G - V_{th}) \tag{24}$$

(Effects of Φ_{MS}, Q'_{ss} and Q'_{ox} are simply included in V_{th} in this equation.)

This is a very important result which we will apply to MOS transistors later.

Subthreshold Conduction



Note that the linear relationship between g_I and $V_G - V_{th}$ agrees with experiment except for V_G very close to V_{th}.

For $V_G \approx V_{th}$ (weak inversion), the relationship between Q'_I and V_G may be shown to be

$$Q'_I \cong -C'_{ox}\Delta V \exp\left(\frac{V_G - V_{th} - \Delta V}{\Delta V}\right) \tag{25}$$

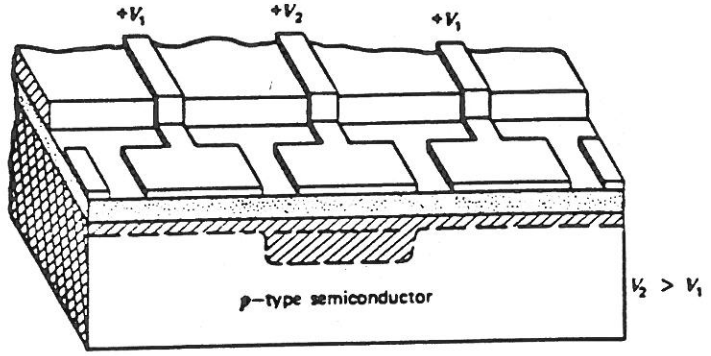
That is, for weak inversion, an exponential relationship between Q'_I and V_G holds.

Intuitively, this behavior arises because the charge varies exponentially with ϕ_s before ϕ_s is effectively "pinned" at $2\phi_F$ from the bulk potential. (electron concentration varies exponentially with ϕ_s from F.D. statistics.)

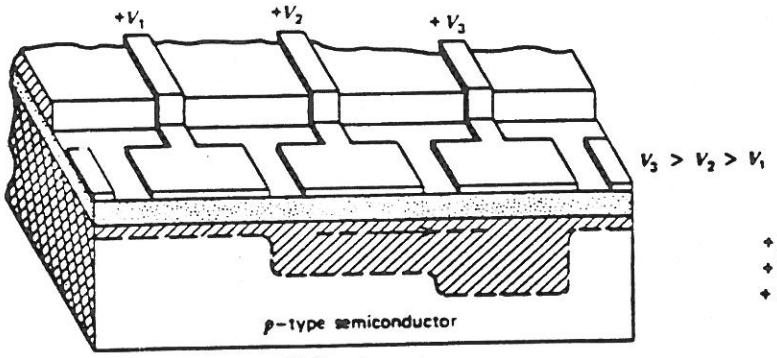
Charge-Coupled Devices

Charge-coupled devices essentially consist of an array of MOS capacitors. The capacitors are close enough together that charge stored in channel of one capacitor can be transferred to the channel of a neighboring capacitor if the gate voltage are modulated properly.

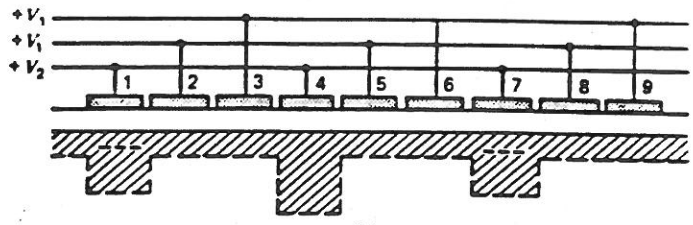
These devices can be used as either high density shift registers, analog delay lines or imaging devices where incident light can be used as the source of generated charges.



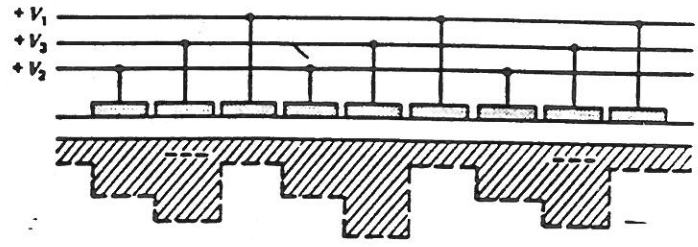
(a) Storage mode



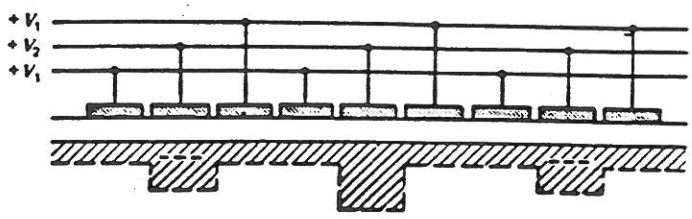
(b) Transfer mode



(a)



(b)



(c)