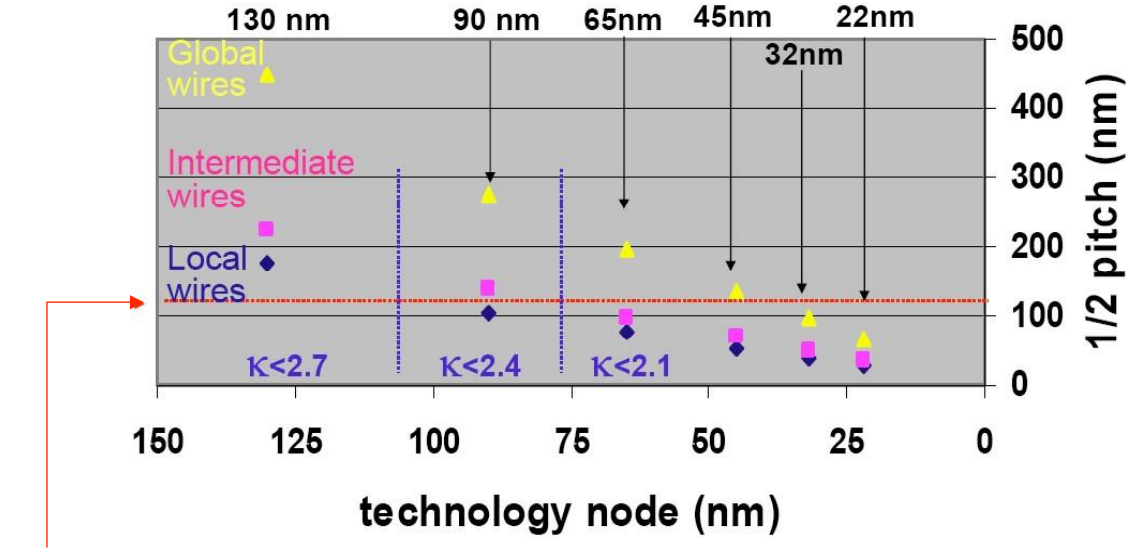
Interconnections: Copper & Low K Dielectrics

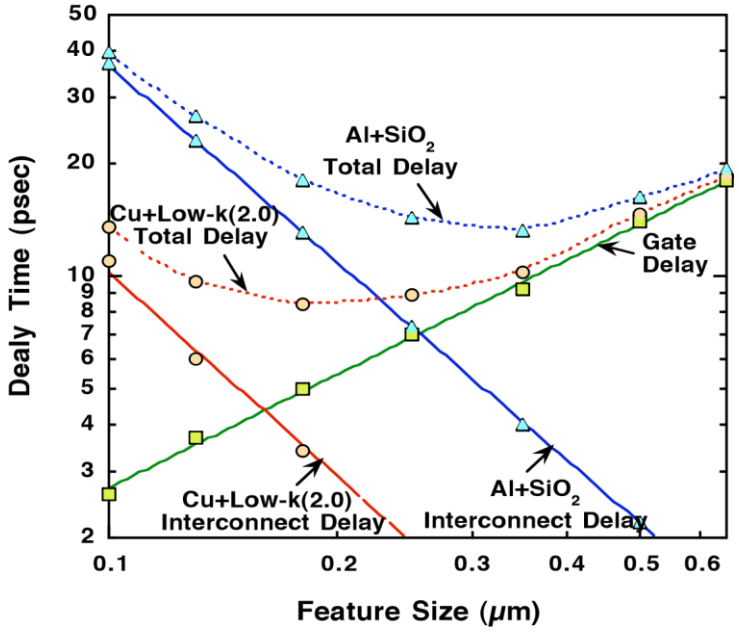
ITRS 2002 Interconnect Scaling Recommendations



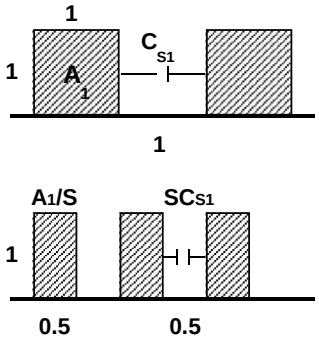
Narrow line effects

Ref: J. Gambino, IEDM Short Course, 2003

Interconnect Scaling Scenarios

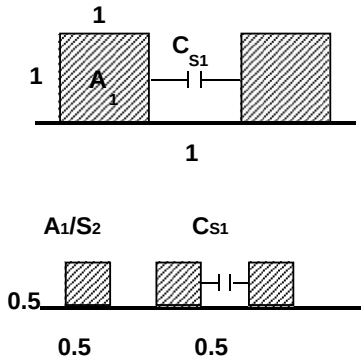


Scaling need for lower resistivity metal, Low-k



- **Scale Metal Pitch and Height**

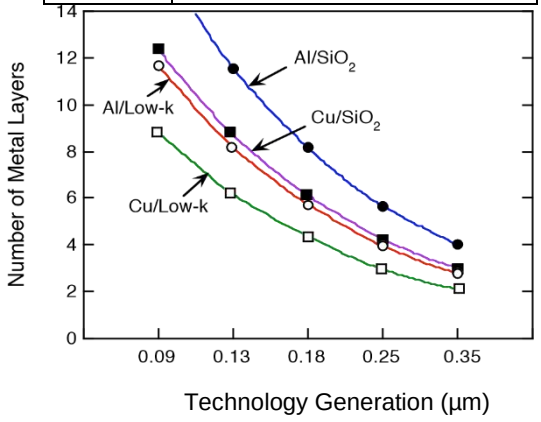
- R and J increase by square of scaling factor
- Sidewall capacitance unchanged
- Aspect ratio for gapfill / metal etch unchanged
- Drives need for very low resistivity metal with significantly improved EM performance



Why Cu?

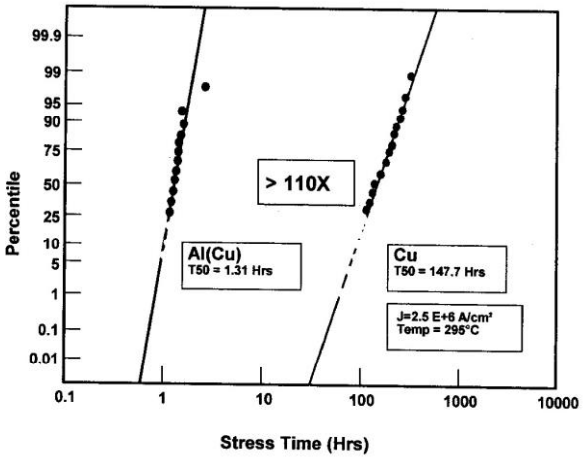
- Lower resistivity than Al or Al alloys - reduced RC delay.

Metal	Bulk Resistivity [!"•cm]
Ag	1.63
Cu	1.67
Au	2.35
Al	2.67
W	5.65



- Better electromigration reliability than Al alloys.

	Al	Cu
Melting Point	**660 ºC**	**1083 ºC**
E_a for Lattice Diffusion	**1.4 eV**	**2.2 eV**
E_a for Grain Boundary Diffusion	**0.4 – 0.8 eV**	**0.7 – 1.2 eV**

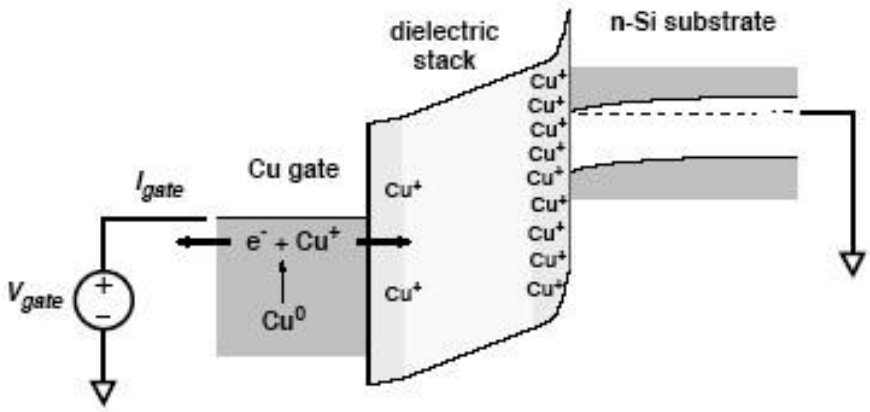


Ref: S. Luce, (IBM), IEEE IITC 1998

Challenges for Cu Metallization

Limited processing methods: Introduction of Cu must be managed carefully.

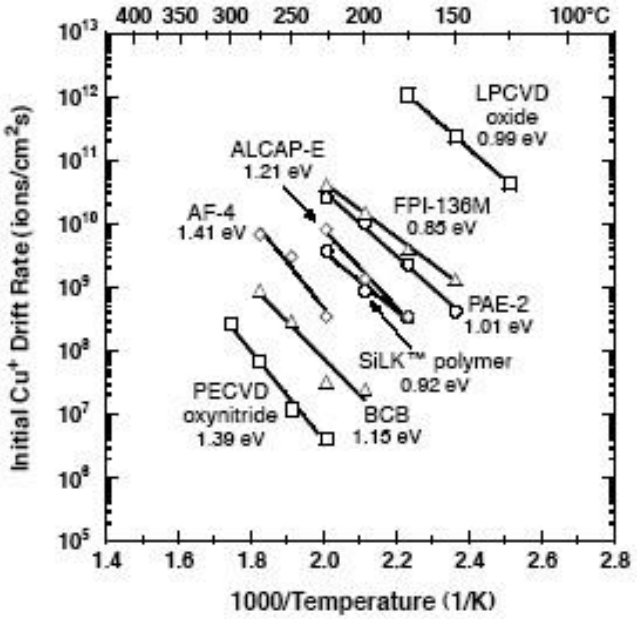
- Obstacles
  - Line patterning: Poor dry-etchability of Cu - Poor adhesion to dielectrics
  - Copper is very mobile in SiO_2 => Contamination to Si Devices
    - Increased leakage in SiO_2
    - Increased junction leakage
    - Lower junction break down voltage



Cu atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as Cu+ space charge.

- Bias temperature stressing is employed to characterize behavior
  - Both field and temperature affect barrier lifetime
  - Neutral Cu atoms and charged Cu ions contribute to Cu transport through dielectrics

- Silicon nitride and oxynitride films are better barriers



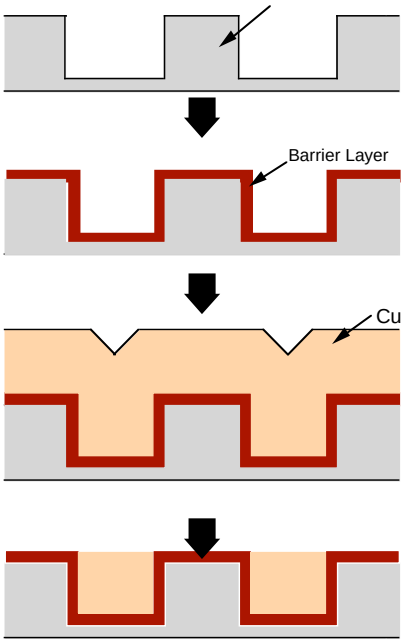
Ref: A. Loke et al., Symp. VLSI Tech. 1998

- **Fast diffusion of Cu into Si and SiO_2**
  Dielectrics
- **Poor oxidation/corrosion resistance**
- **Poor adhesion to SiO_2**

Diffusion barrier /adhesion promotor
Passivation

- **Difficulty of applying conventional dry-etching technique**

Damascene Process

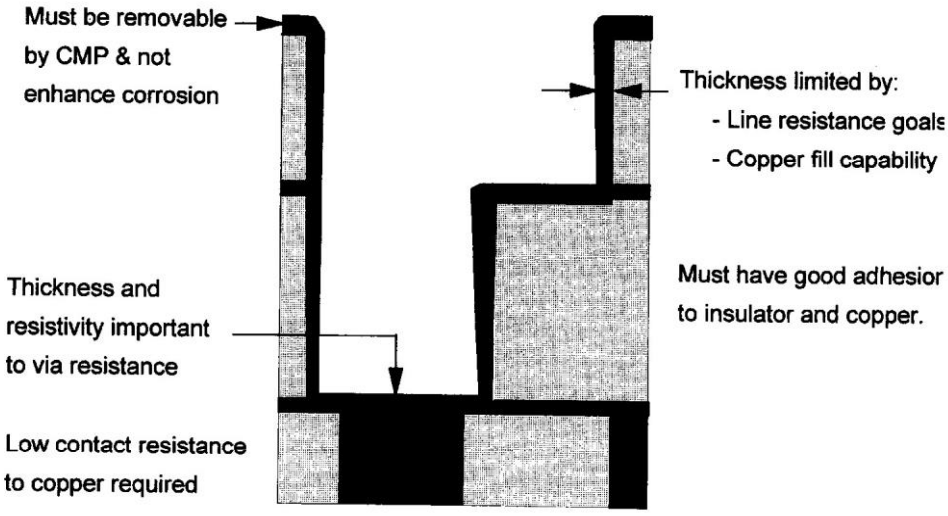


Typical Damascene Process

Solutions

- Damascene process for patterning
- Using diffusion Barriers
  - Liners TiN, TaN, etc
  - Silicon Nitride, PSG
  -

Barriers/Liners



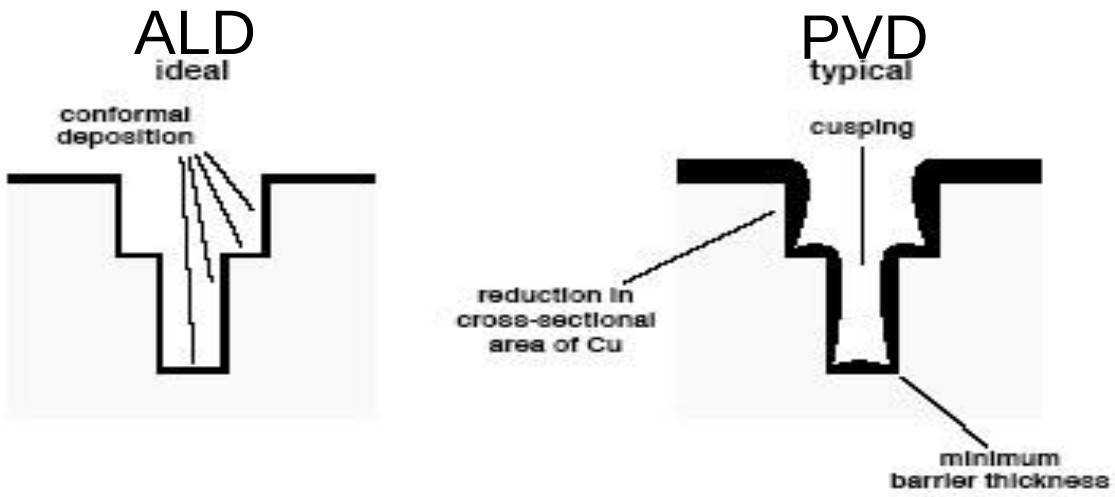
Barrier Requirements:

- Ultrathin films should be good barriers
- Low resistance
- Chemically stable
- Defect free to high temperatures

Barriers:

- Transition metals (Pd, Cr, Ti, Co, Ni, Pt) generally poor barriers, due to high reactivities to Cu <450˚*C*
  - Exception: Ta, Mo, W ... more thermally stable, but fail due to Cu diffusion through grain boundaries (polycrystalline films)
- Transition metal alloys: Can be deposited as amorphous films (stable up to 500˚C)
- Transition metal - silicon compounds: Adding Si to Ta, Ti, Mo, W yields amorphous refractory barriers with stability to 700˚C
- Amorphous ternary alloys: Very stable due to high crystallization temperatures (i.e., $Ta_{36}S_{14},N_{50}$, $Ti_{34}Si_{23}N_{43}$)

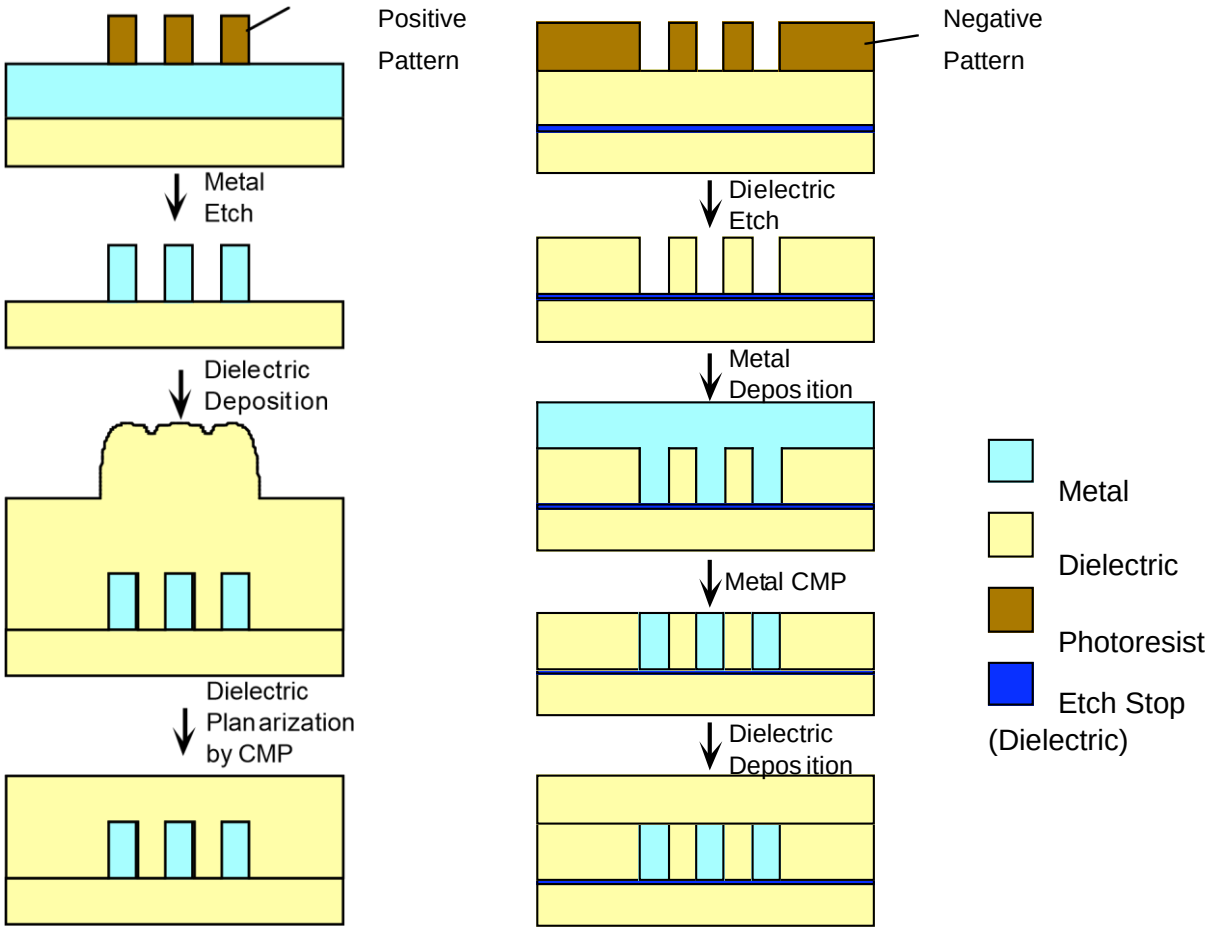
- Currently PVD (sputtering/evaporation is used primarily to deposit the barrier/liner, however, step coverage is a problem. ALD is being developed for barrier/liner application.



Interconnect Fabrication Options

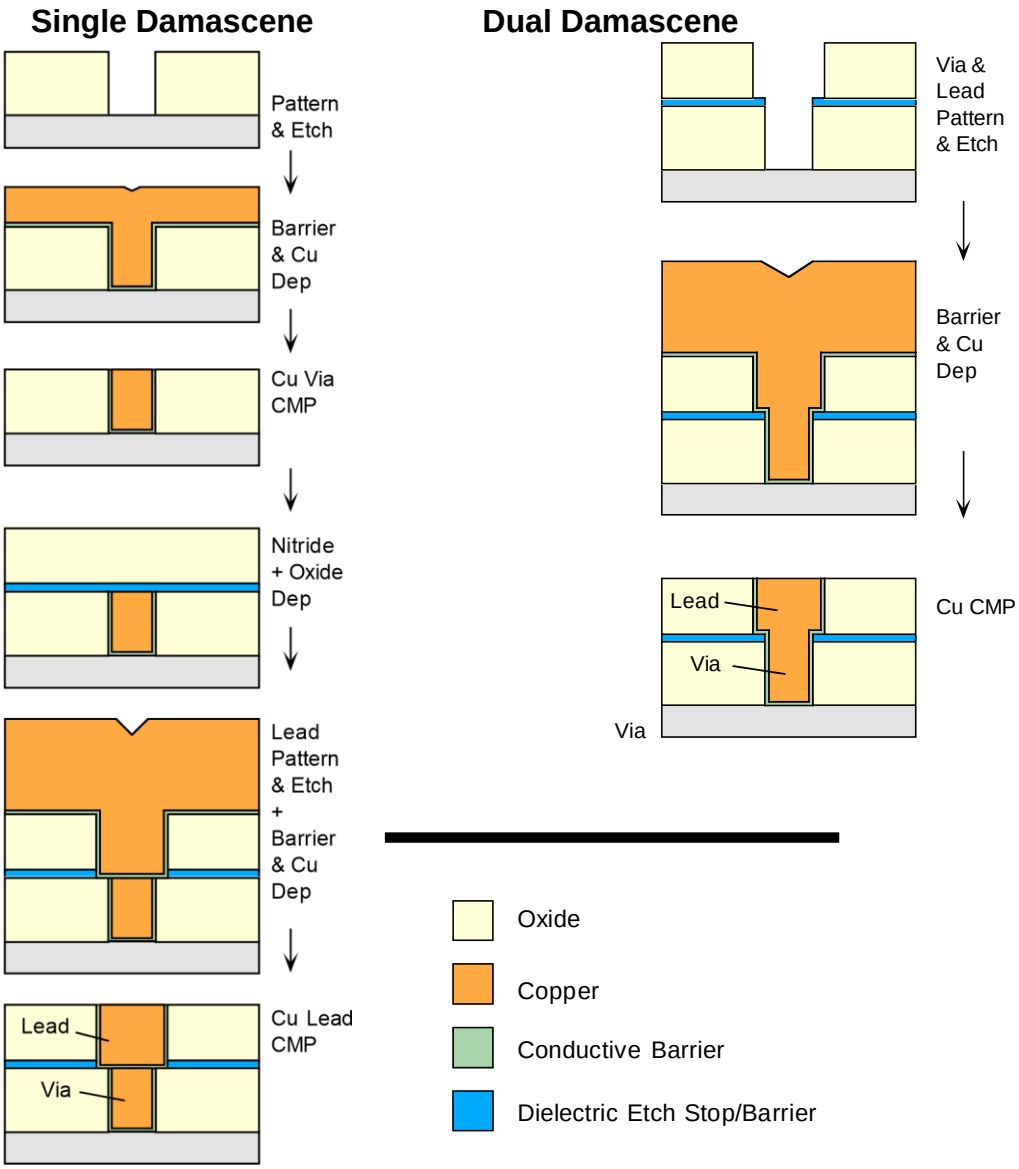
Subtractive Etch
(Conventional Approach)

Damascene



- Conventional approach of metal etch is used for Al
- Damascene approach is used for Cu as it can't be dry etched

Cu Damascene Flow



Deposition methods

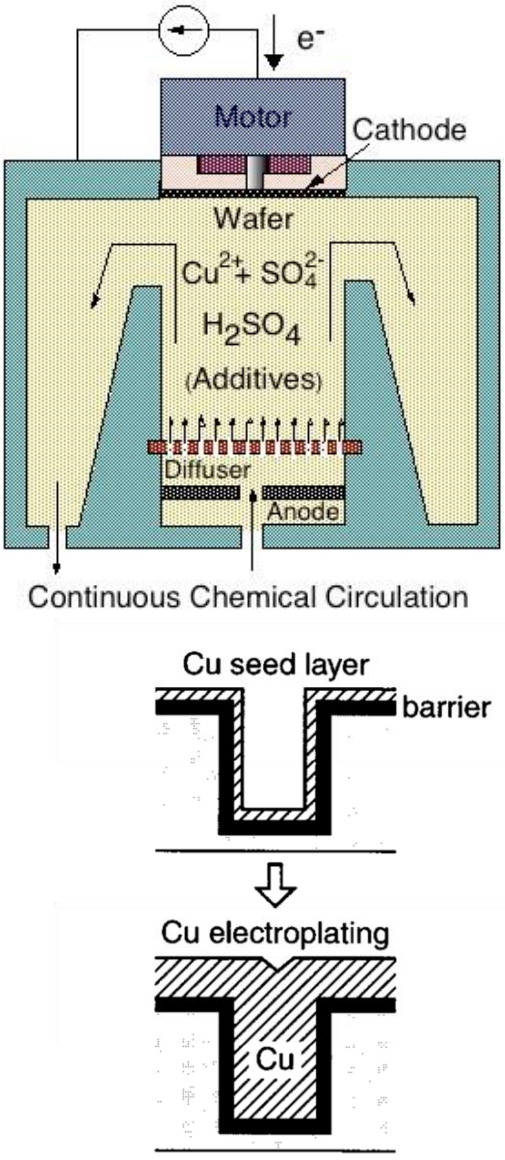
Physical vapor deposition (PVD) : Evaporation, Sputtering

- conventional metal deposition technique: widely used for Al interconnects
- produce Cu films with strong (111) texture and smooth surface, in general
  - poor step coverage: not tolerable for filling high-aspect ratio features

Chemical vapor deposition (CVD) :

- conformal deposition with excellent step coverage in high-aspect ratio holes and vias
- costly in processing and maintenance
- generally produce Cu films with fine grain size, weak (111) texture and rough surface

Electroplating System for Cu



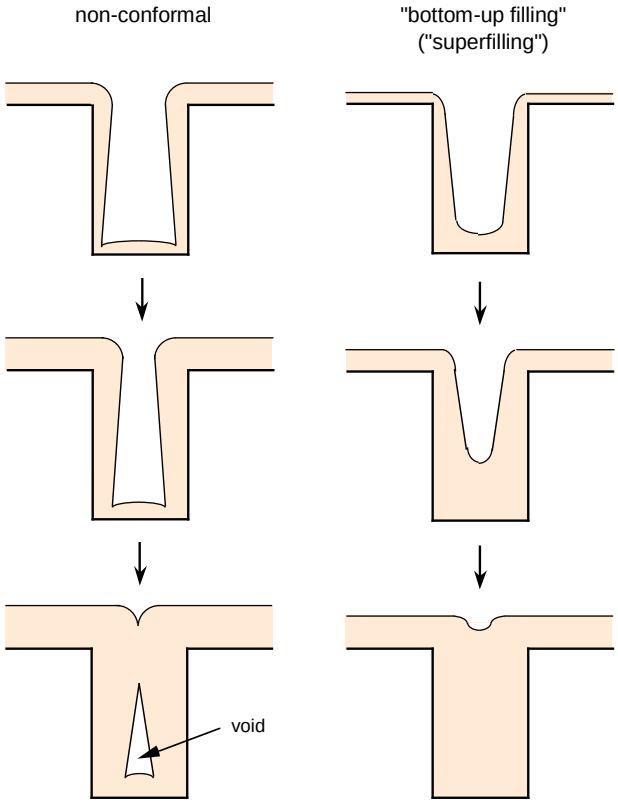
Dissociation: $CuSO_4 \rightarrow Cu^{2+} + SO_4^{2-}$ (solution)

Reduction: $Cu^{2+} + 2e^- \rightarrow Cu$ (cathode)

Oxidation: $Cu \rightarrow Cu^{2+} + 2e^-$ (anode)

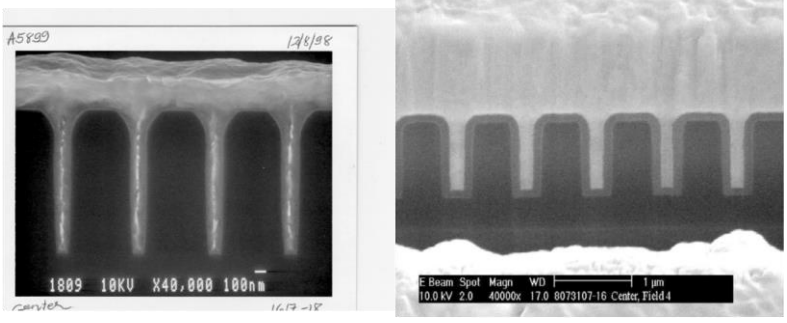
- Direct electroplating on the barrier gives poor results. Therefore a thin layer of Cu is needed as a seed. It can be deposited by PVD, CVD or ALD.
- Good step coverage and filling capability comparable to CVD process (0.25 μm)
- Compatible with low-K dielectrics
- Generally produce strong (111) texture of Cu film
- Produce much larger sized grain structure than any other deposition methods through self-annealing process

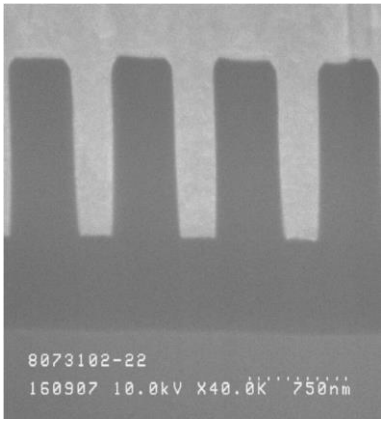
Trench Filling PVD vs. Electroplating of Cu



PVD **Electroplating Trench**

Filling Capability of Cu Electroplating





0.13µ trenches **0.18µ vias** **029µ vias**

Ref: Jonathan Reid, IITC, 1999