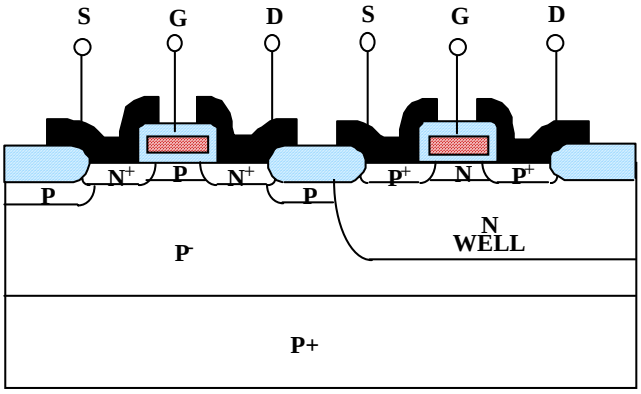
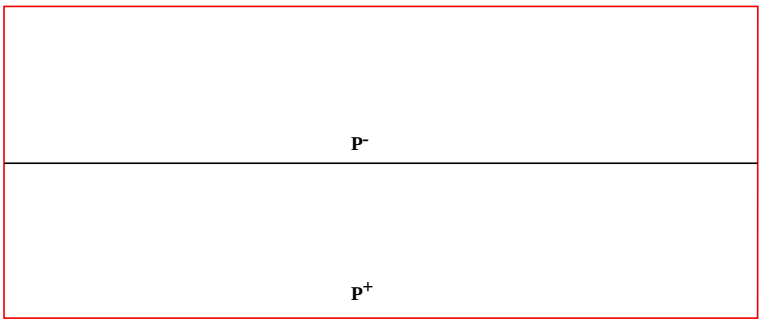
2.1 Sketch a process flow that would result in the structure shown in Figure 1-34 by drawing a series of drawings similar to those in this chapter. You only need to describe the flow up through the stage at which active device formation starts since from that point on, the process is similar to that described in this chapter.

Answer:

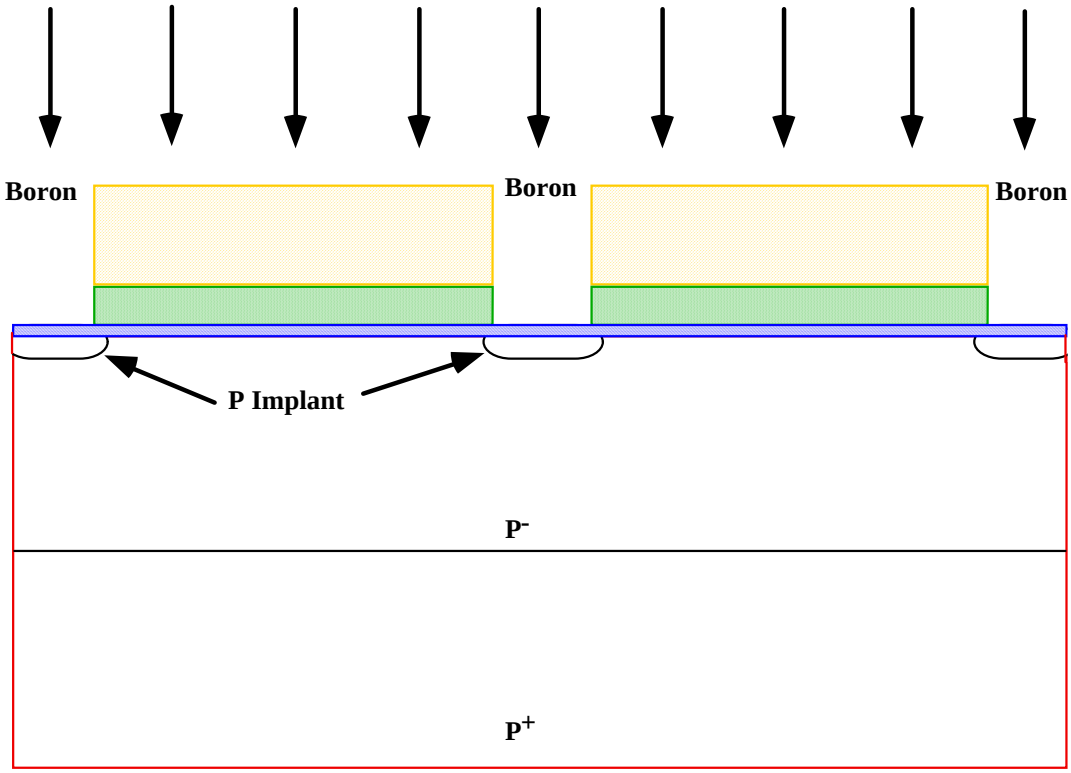
The CMOS technology we need to realize is shown below, from Figure 1-34 in the text.



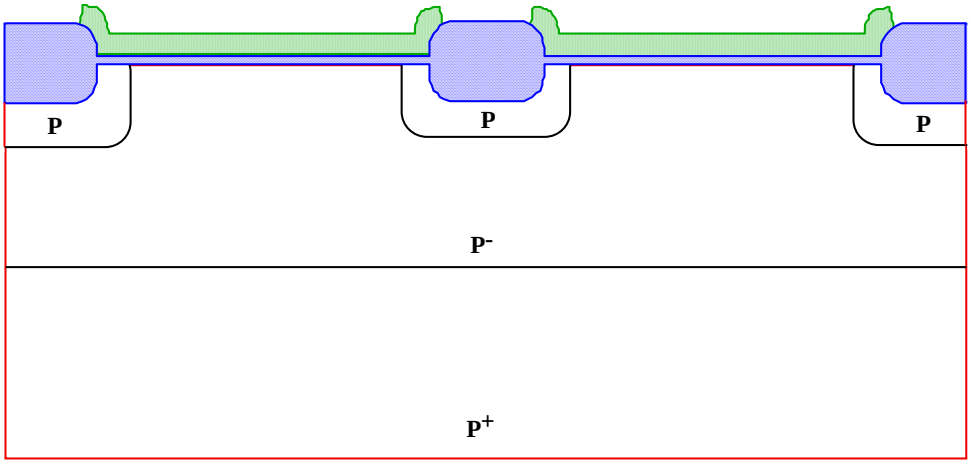
We can follow many of the process steps used in the CMOS process flow in Chapter 2. The major differences are that an epi layer is needed, only one well (P well) used, and the device structures are considerably simplified from those in the text because there are no LDD regions etc.



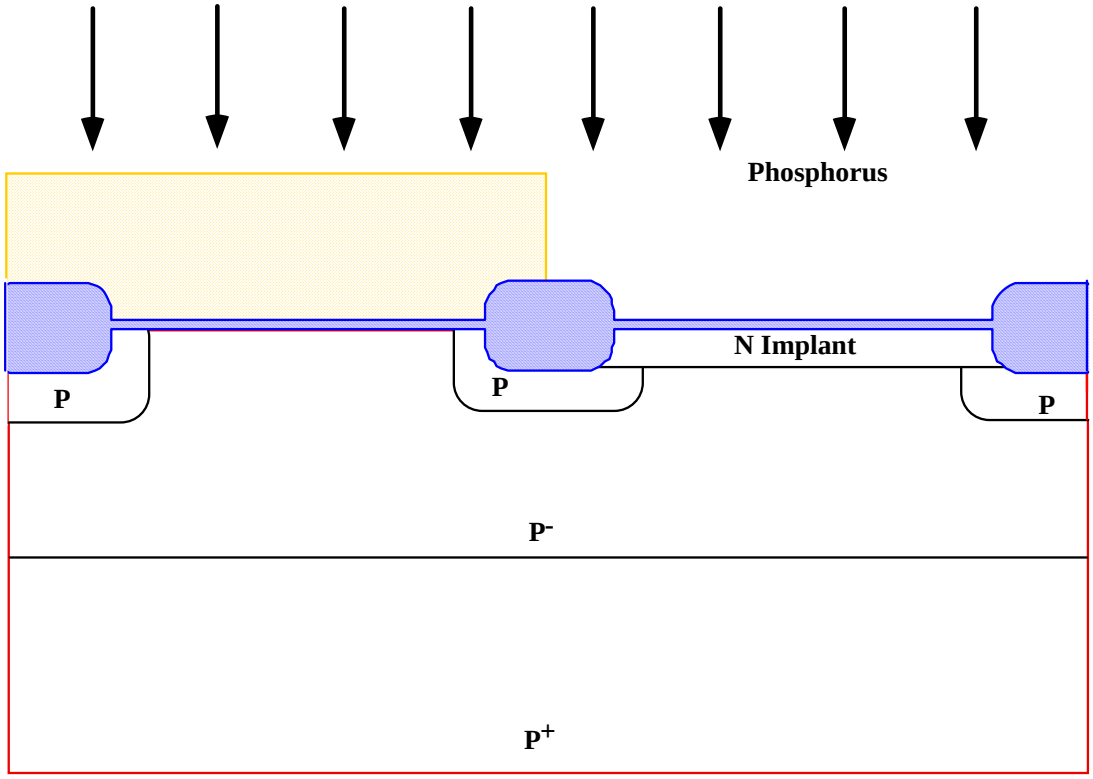
The first step is to grow the blanket epi layer shown in the final cross-section. A heavily doped P^+ substrate is chosen and a lightly doped boron epitaxial layer is grown uniformly on its surface.



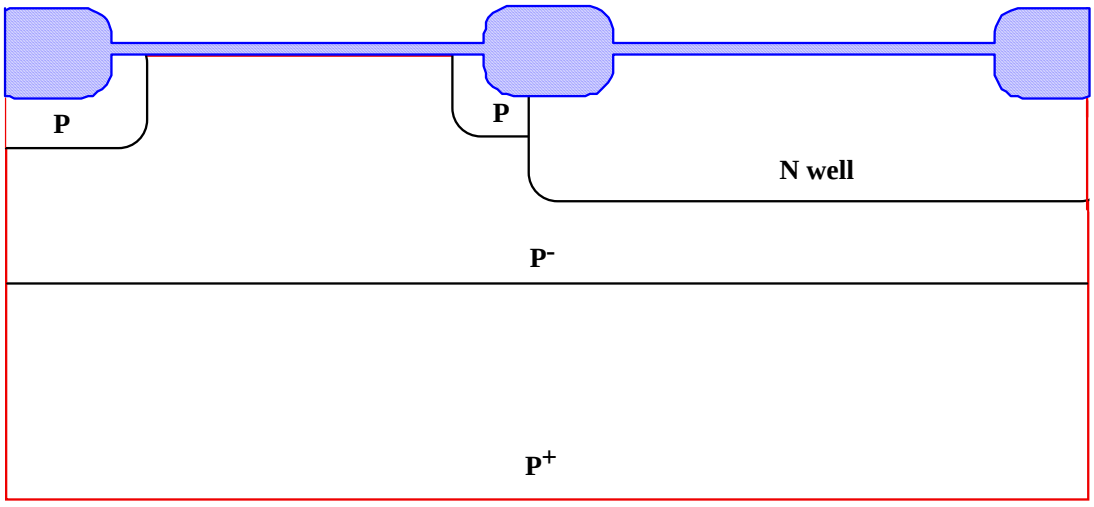
Mask #1 patterns the photoresist. The Si_3N_4 layer is removed where it is not protected by the photoresist by dry etching.Since the technology uses field implants below the field oxide, a boron implant is used to dope these P regions.



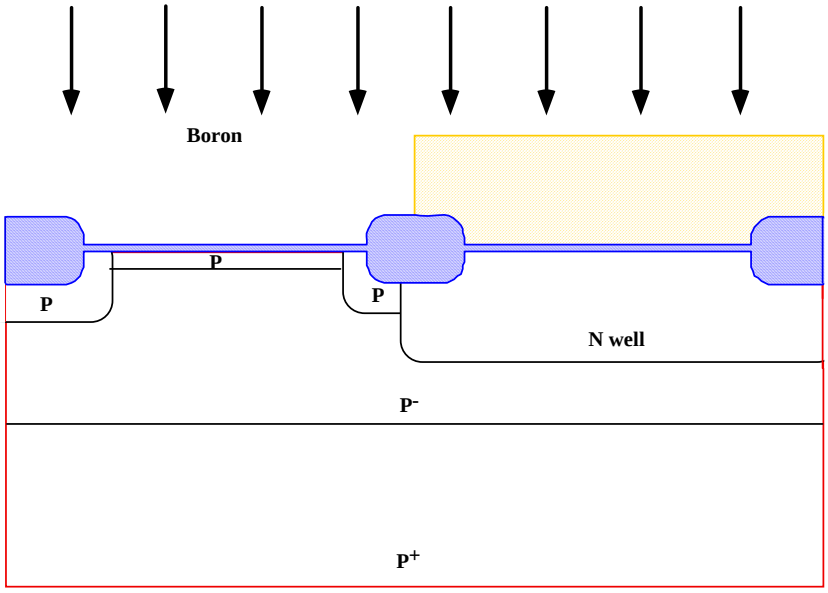
During the LOCOS oxidation, the boron implanted regions diffuse ahead of the growing oxide producing the P doped regions under the field oxide. The Si_3N_4 is stripped after the LOCOS process.



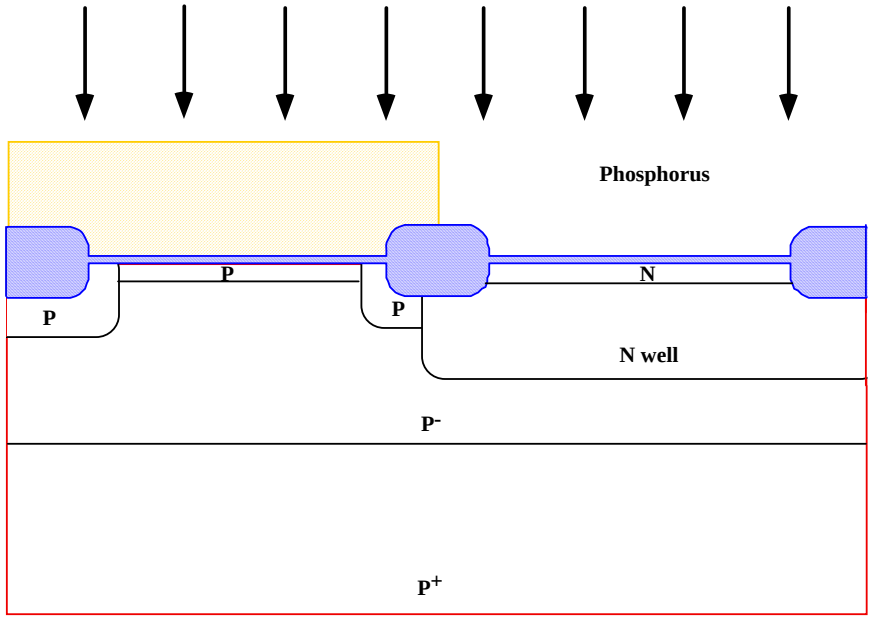
Mask #2 is used to form the N well. Photoresist is used to mask the regions where NMOS devices will be built. A phosphorus implant provides the doping for the N wells for the PMOS devices



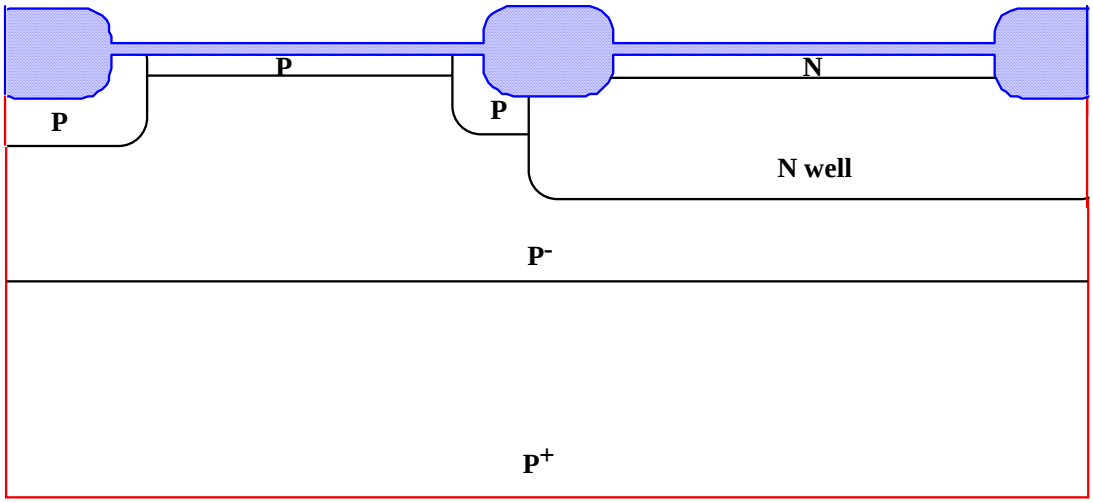
A high temperature drive-in completes the formation of the N well.



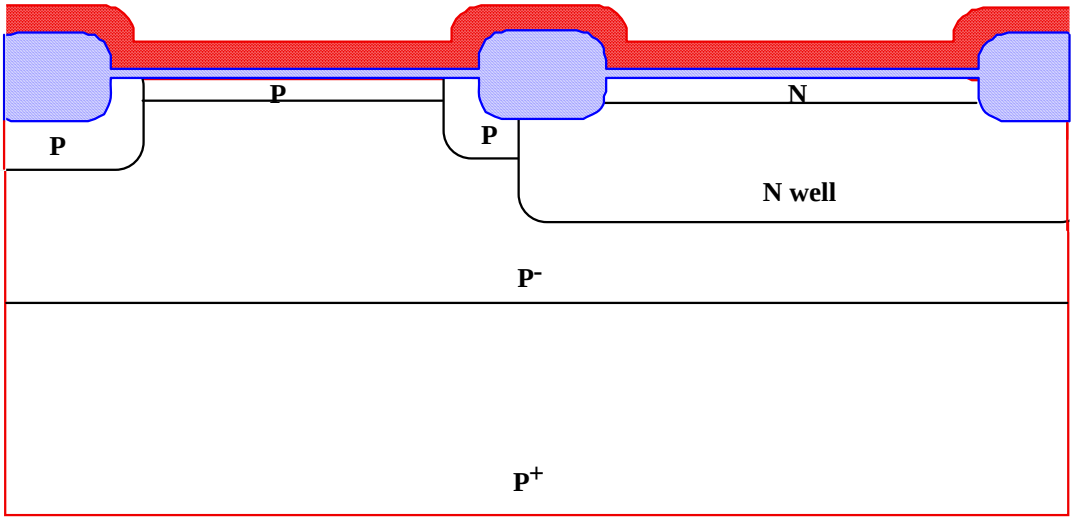
After spinning photoresist on the wafer, mask #3 is used to define the NMOS transistors. A boron implant adjusts the N channel V_{TH}.



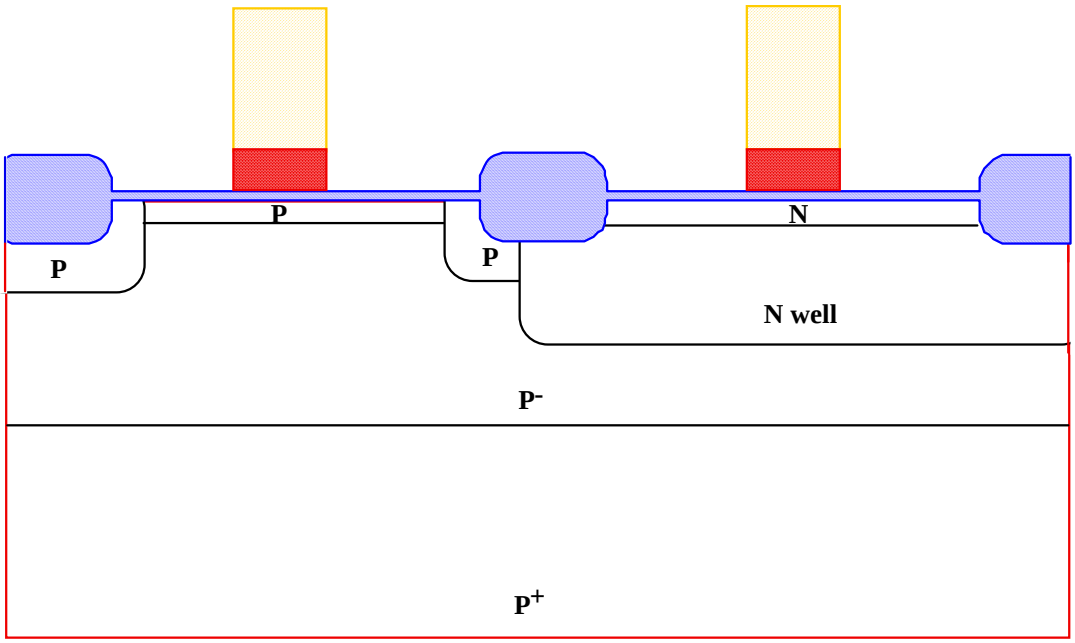
After spinning photoresist on the wafer, mask #4 is used to define the PMOS transistors. A phosphorus or arsenic implant adjusts the P channel V_{TH}. (Depending on the N well doping, a boron implant might actually be needed at this point instead of an N type implant, to obtain the correct threshold voltage.)



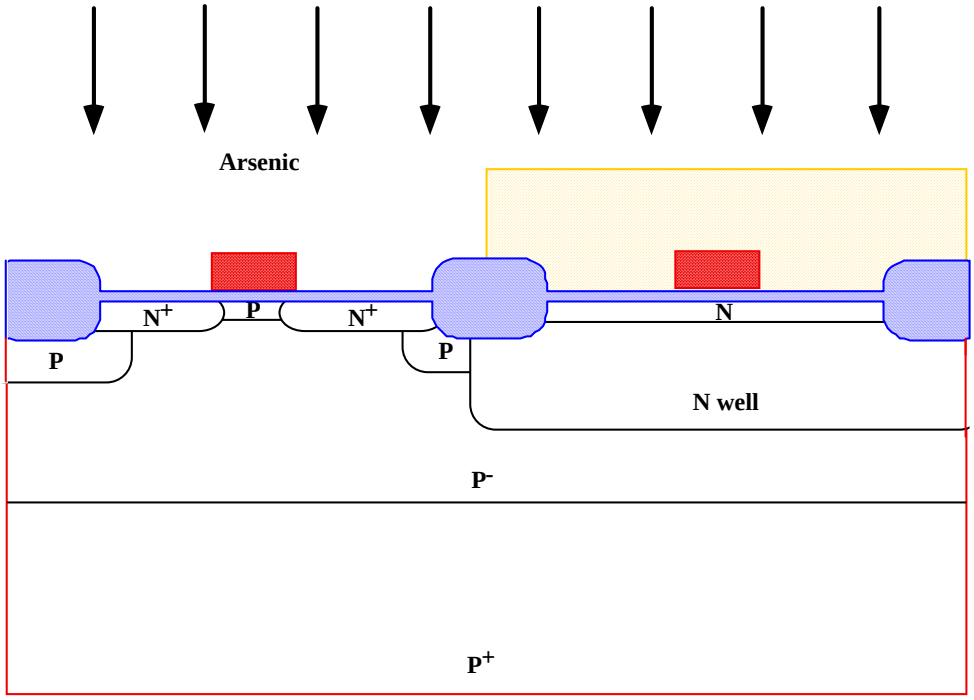
After etching back the thin oxide to bare silicon, the gate oxide is grown for the MOS transistors.



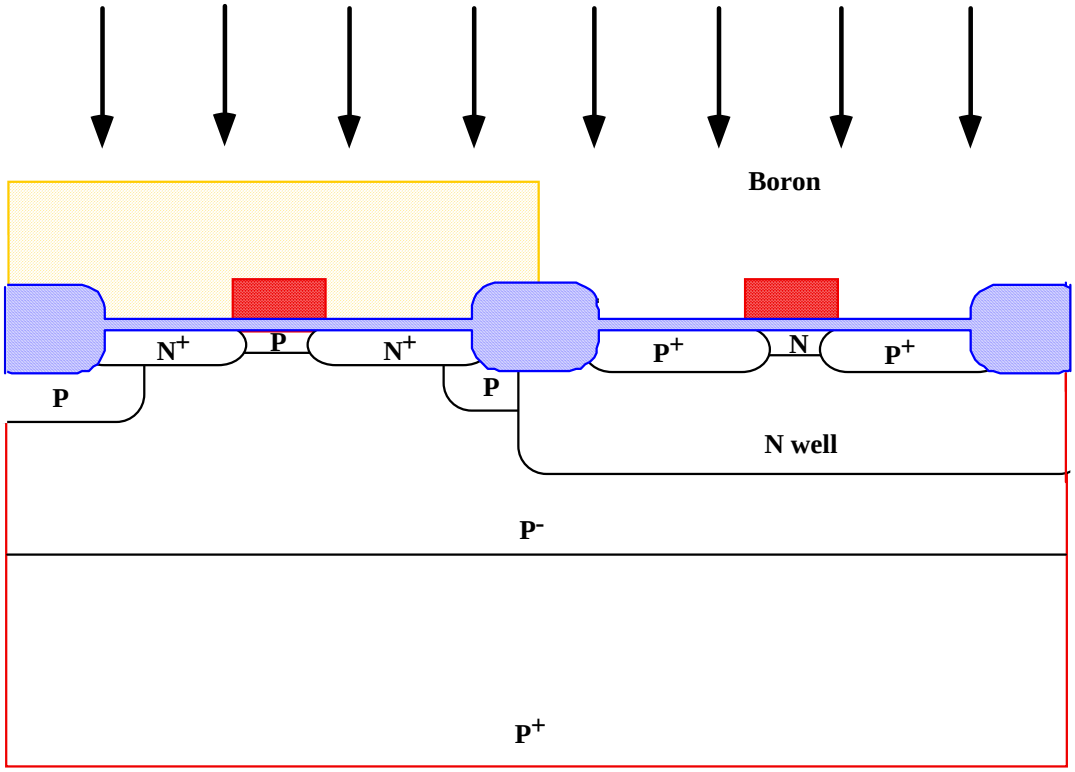
A layer of polysilicon is deposited. Ion implantation of phosphorus follows the deposition to heavily dope the poly.



Photoresist is applied and mask #5 is used to define the regions where MOS gates are located. The polysilicon layer is then etched using plasma etching.



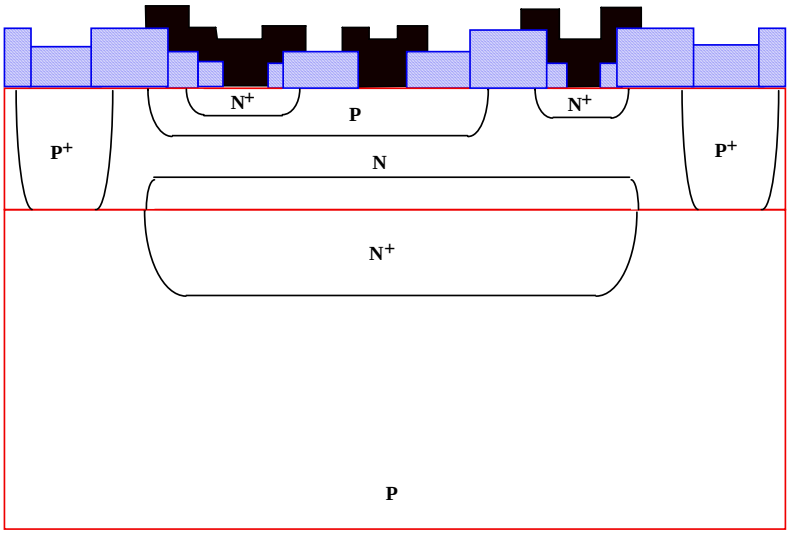
Photoresist is applied and mask #6 is used to protect the PMOS transistors. An arsenic implant then forms the NMOS source and drain regions.



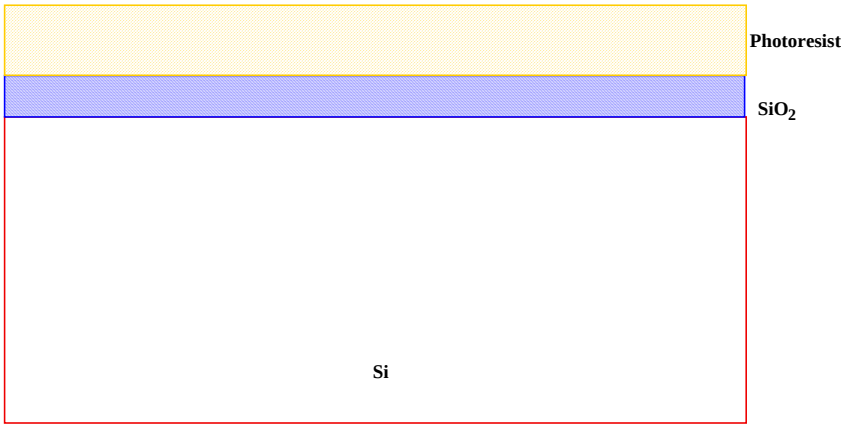
After applying photoresist, mask #7 is used to protect the NMOS transistors. A boron implant then forms the PMOS source and drain regions.

At this point we have completed the formation of the active devices, except for a final high temperature anneal to activate the dopants and drive in the junctions to their final depth. The rest of the process flow would be similar to the CMOS flow in the text.

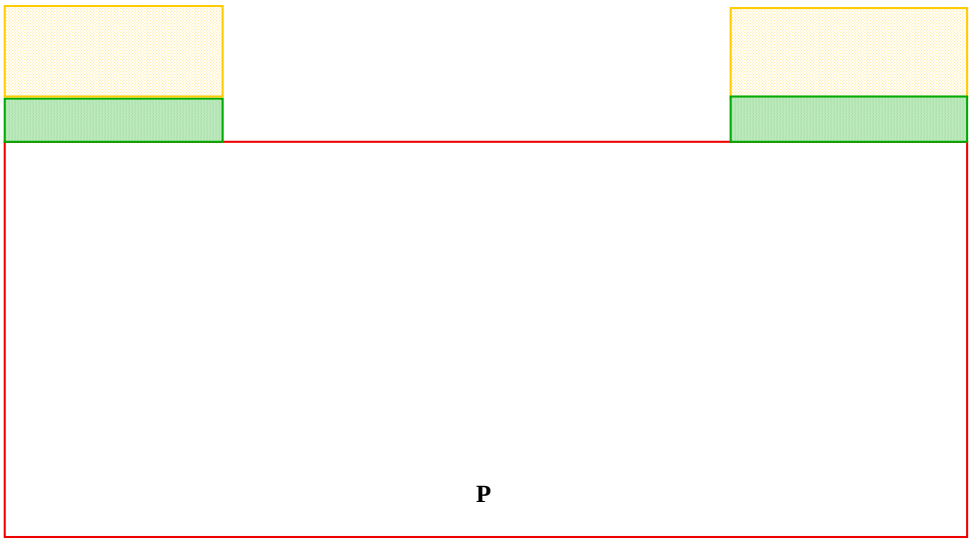
2.3. The cross-section below illustrates a simple bipolar transistor fabricated as part of a silicon IC. (See also Figure 1-32.) Design a plausible process flow to fabricate such a structure, following the ideas of the CMOS process flow in this chapter. You do not have to include any quantitative process parameters (times, temperatures, doses etc.) Your answer should be given in terms of a series of sketches of the structure after each major process step, like the figures in this chapter. Briefly explain your reasoning for each step and the order you choose to do things.



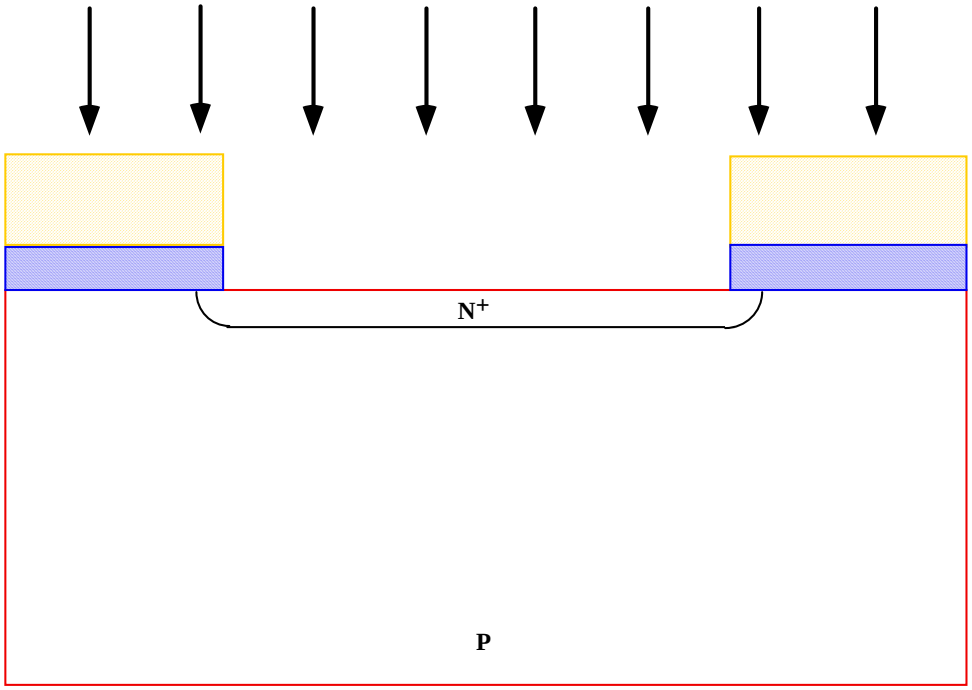
Answer:



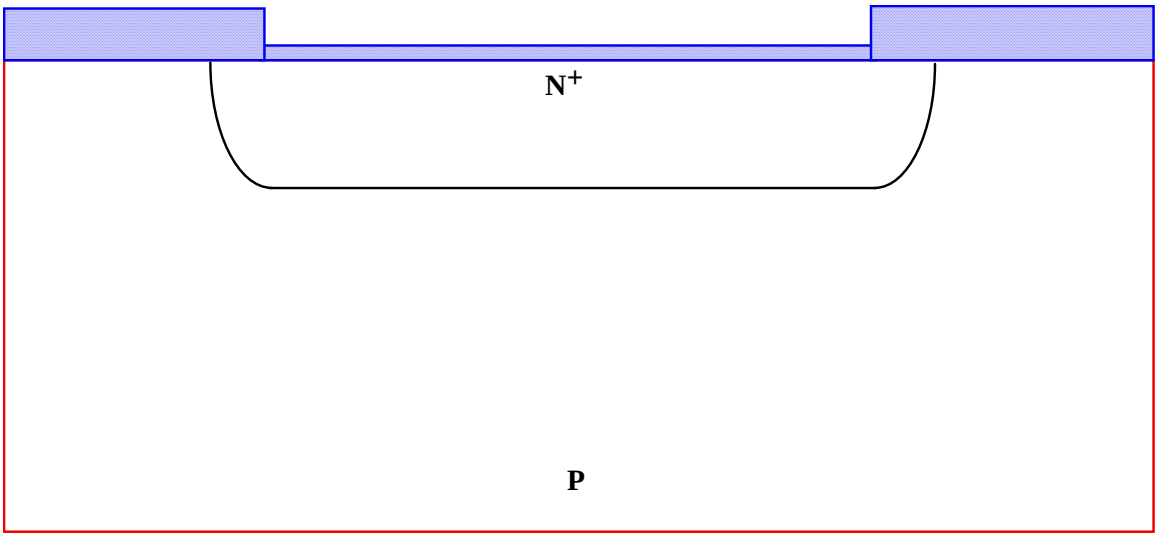
Following initial cleaning, an SiO_2 layer is thermally grown on the silicon substrate. Photoresist is spun on the wafer to prepare for the first masking operation.



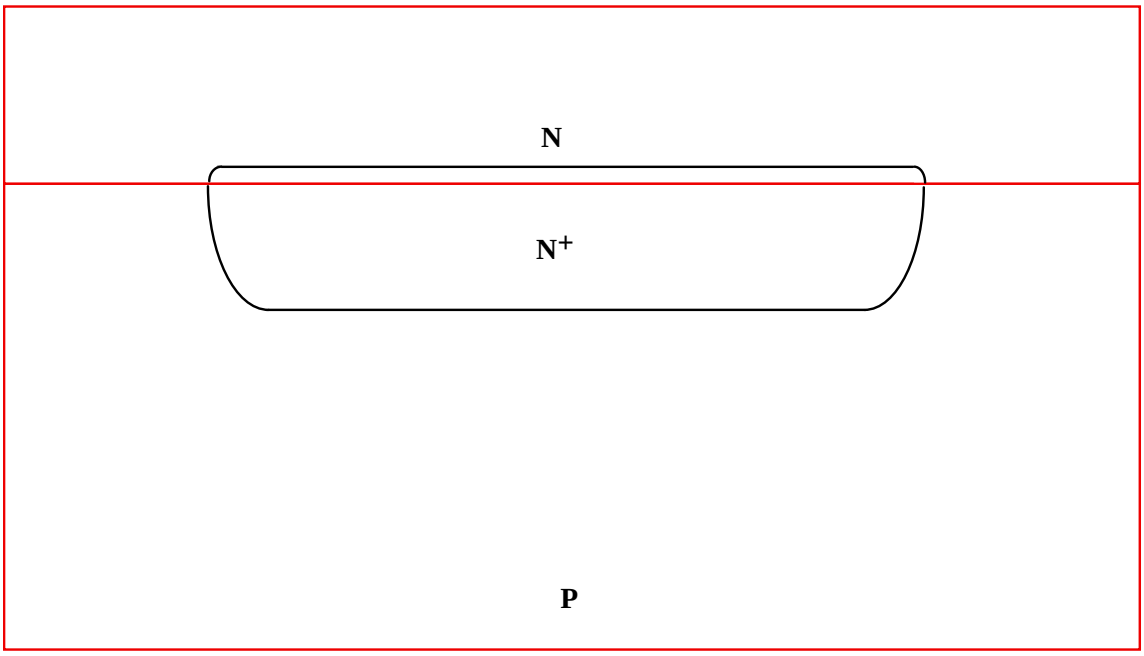
Mask #1 patterns the photoresist. The SiO_2 layer is removed where it is not protected by the photoresist by dry etching.



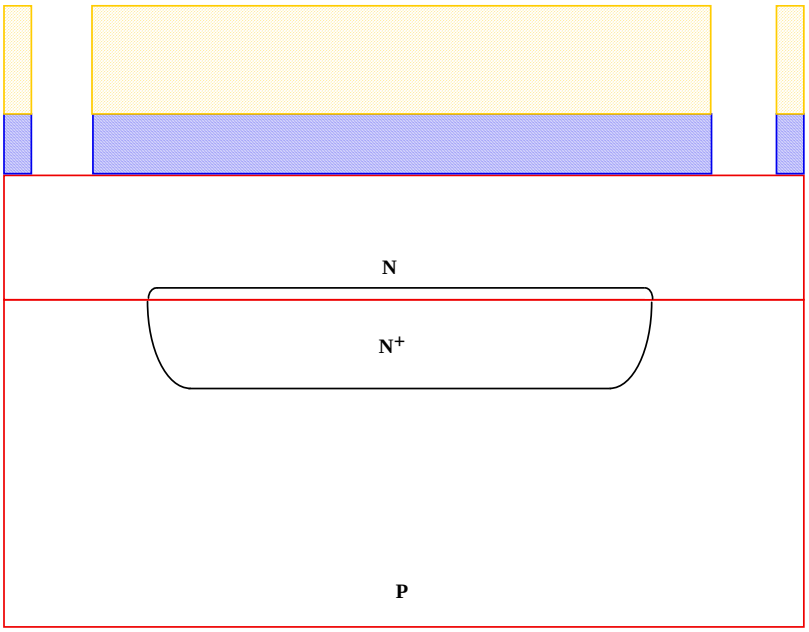
An N^+ implant is performed to dope the buried layer region. As or Sb would typically be used here because they have smaller diffusivities than P.



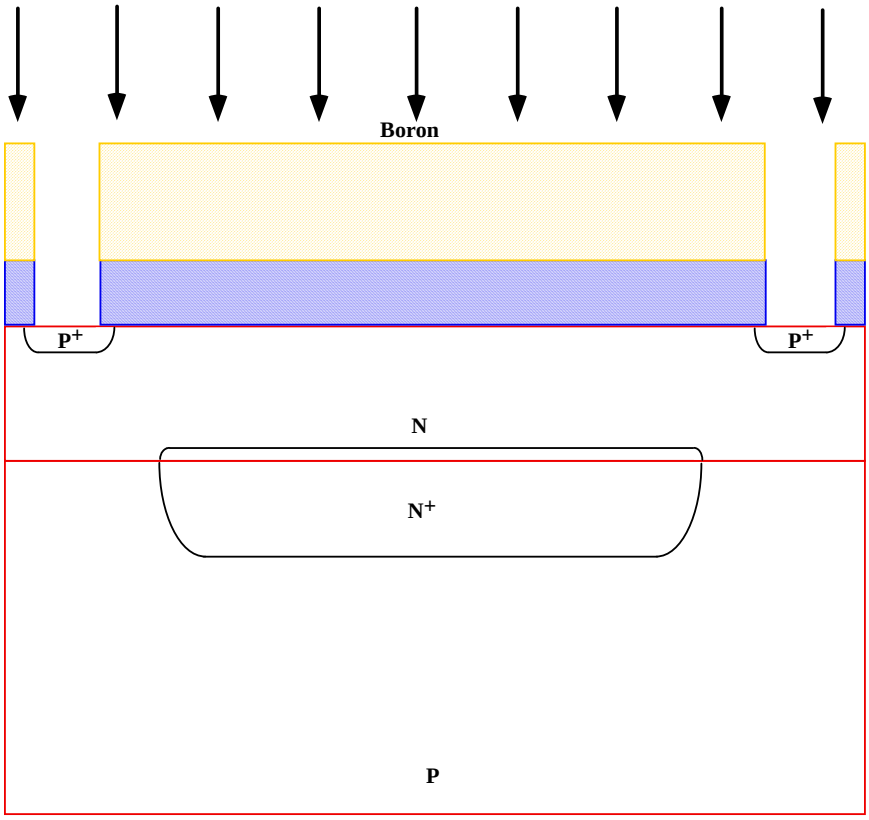
The buried layer is driven in using a high temperature furnace cycle.



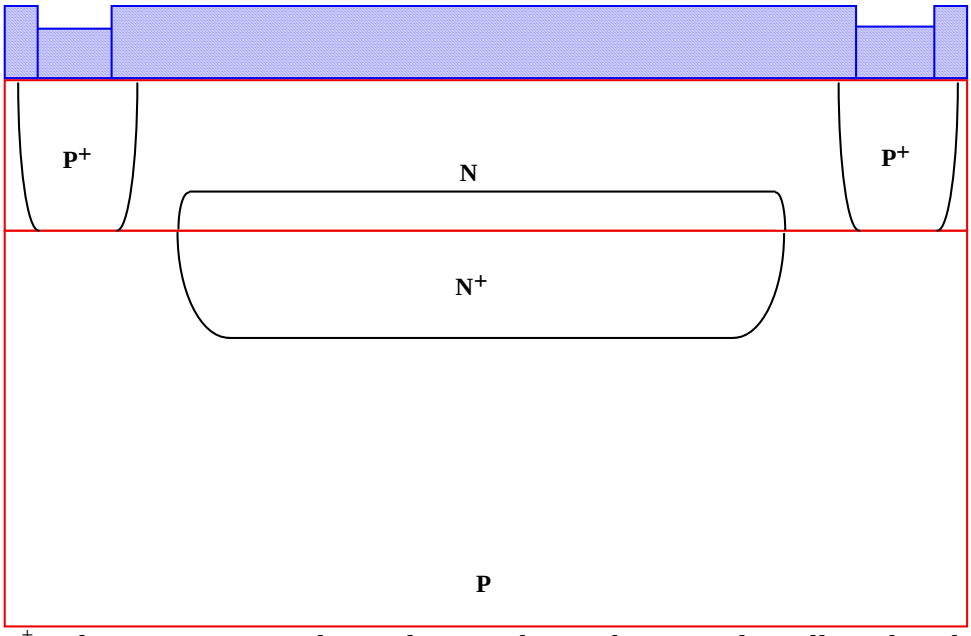
The SiO_2 is etched off the surface and an N type epitaxial layer is grown. Note that during the epi growth, the buried layer diffuses upwards.



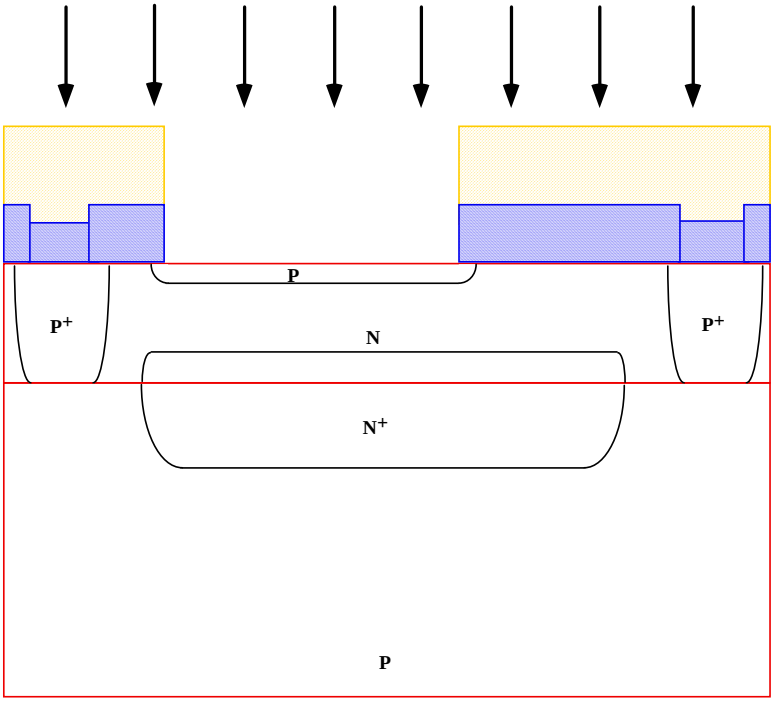
SiO_2 is thermally grown on the surface and photoresist is spun on. Mask #2 is used to define the resist and then the SiO_2 layer is etched using the resist as a mask.



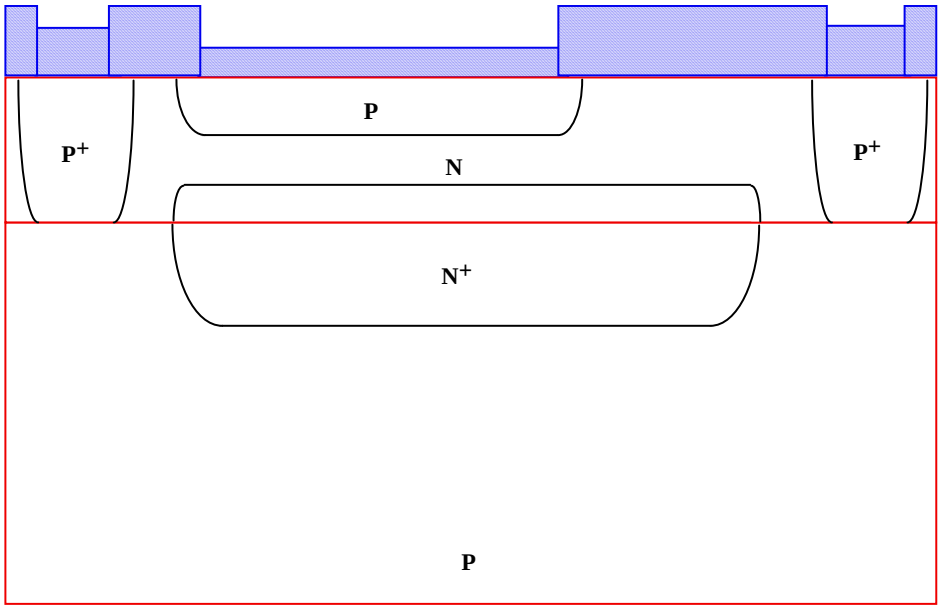
A boron implant dopes the isolation regions.



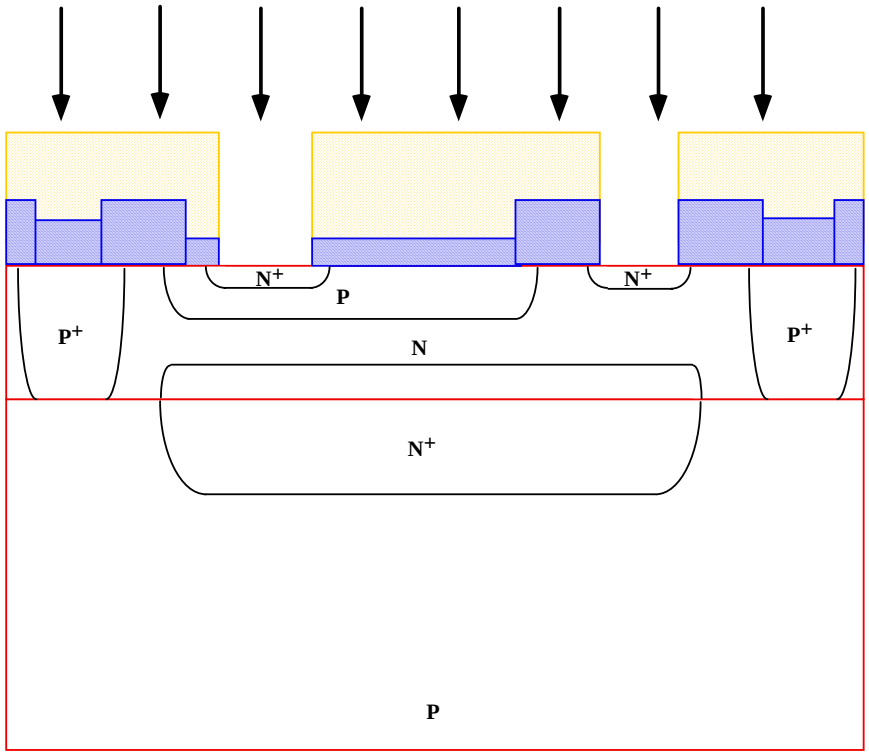
The P^+ isolation regions are driven down to the P substrate to laterally isolate the devices. SiO_2 is grown on the surface during this drive-in. Note that the buried layer continues to diffuse upwards during this high temperature step.



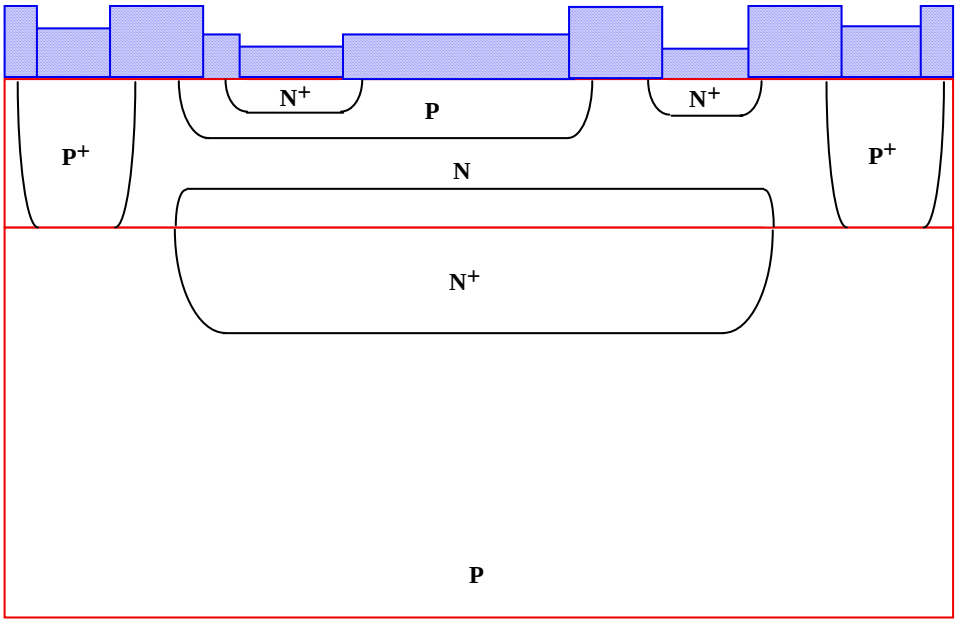
Photoresist is spun onto the wafer and mask #3 is used to define the base regions. The SiO_2 is etched and a boron implant forms the base region.



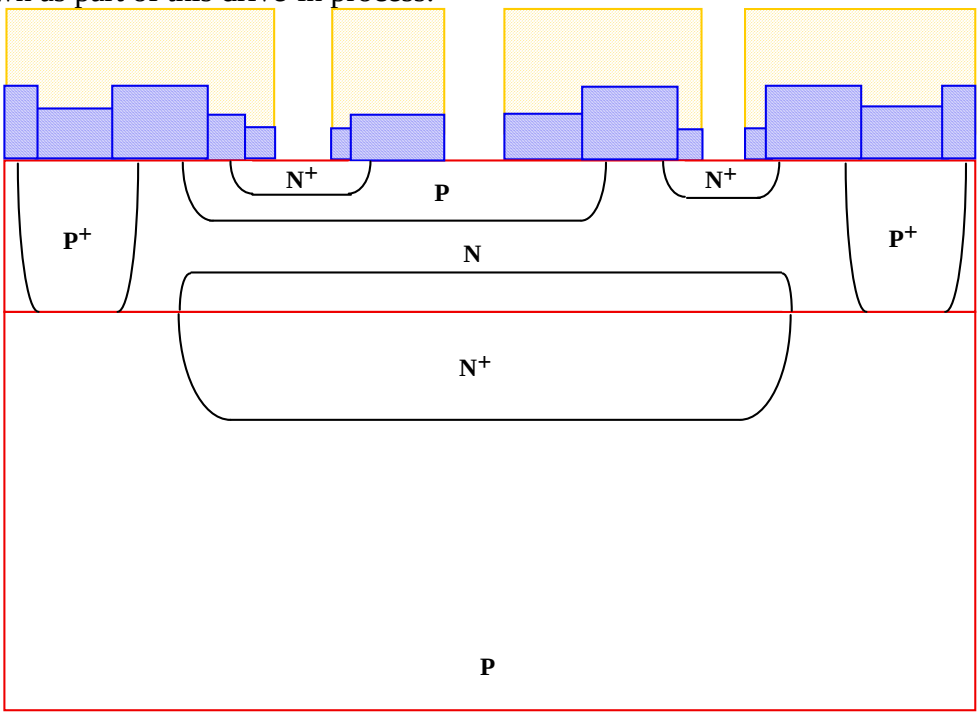
The base region is driven-in to its final junction depth. A surface SiO_2 layer is grown as part of this drive-in process.



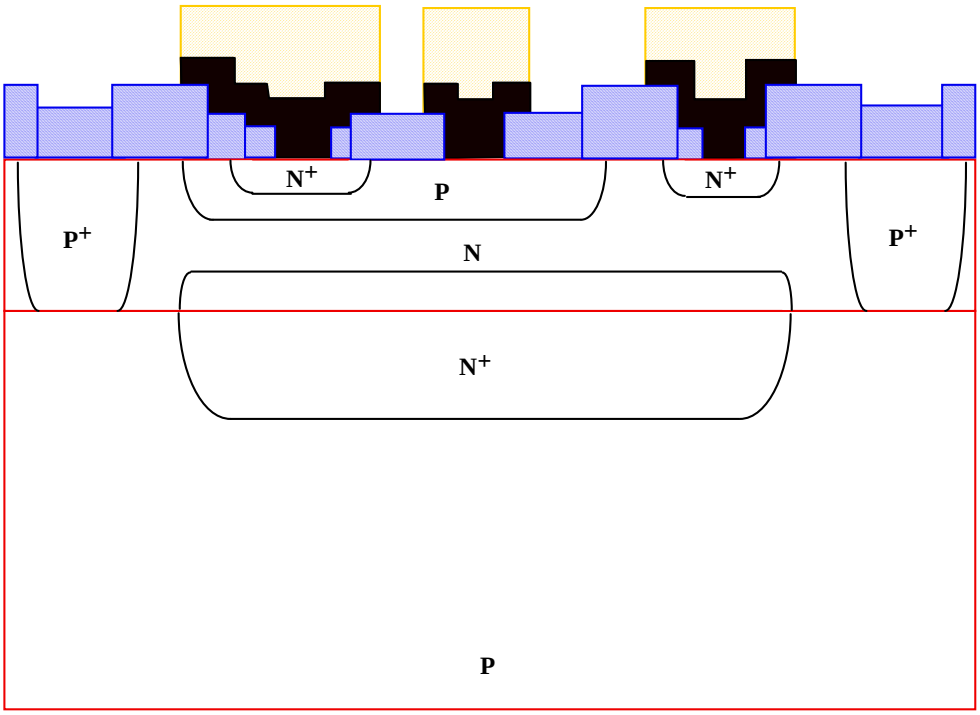
Photoresist is spun onto the wafer and mask #4 is used to define the emitter and collector contact regions. The SiO_2 is etched and an arsenic implant forms the N^+ regions.



The N^+ regions are driven-in to their final junction depth. A surface SiO_2 layer is grown as part of this drive-in process.



Photoresist is spun onto the wafer and mask #5 is used to define the contact regions. The SiO_2 is etched.



Aluminum is deposited on the wafer. Photoresist is then spun onto the wafer and mask #6 is used to define the wiring regions. The Al is then etched. Stripping the photoresist completes the overall process flow.