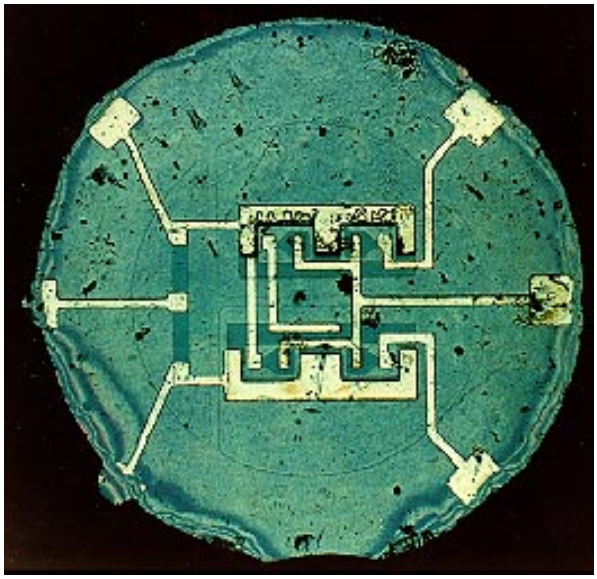
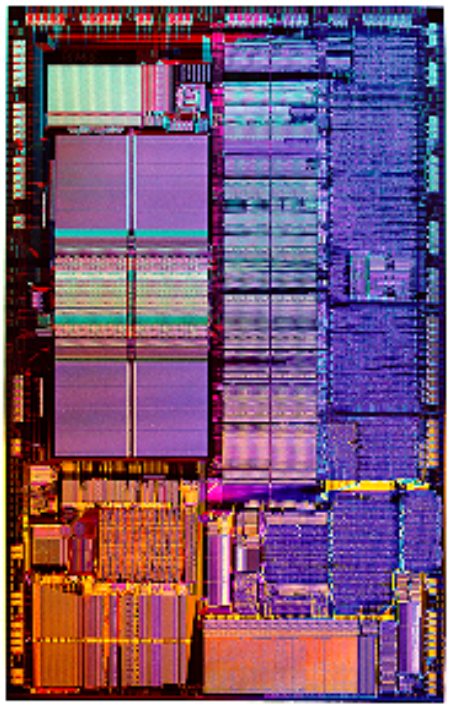
EE 212 FALL 1999-00

- This course is basically about silicon chip fabrication, the technologies used to manufacture ICs.
- We will place a special emphasis on computer simulation tools to help understand these processes and as design tools.
- These simulation tools are more sophisticated in some technology areas than in others, but in all areas they have made tremendous progress in recent years.

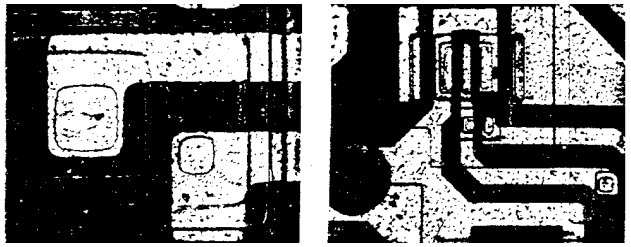
INTRODUCTION - Chapter 1 in the Text



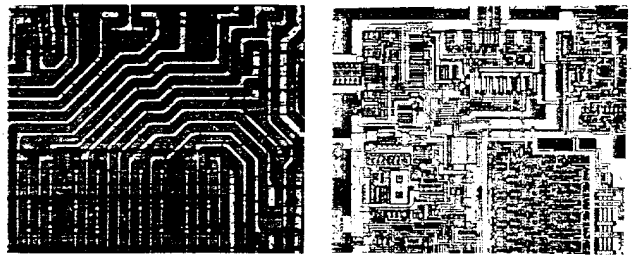


- 1960s and early 1990s integrated circuits.

- Progress due to:
  - Feature size reduction - 0.7X/3 years (Moore's Law).
  - Increasing chip size - ≈ 16% per year.
  - "Creativity" in implementing functions.

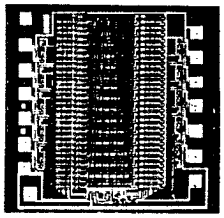


1961 1965

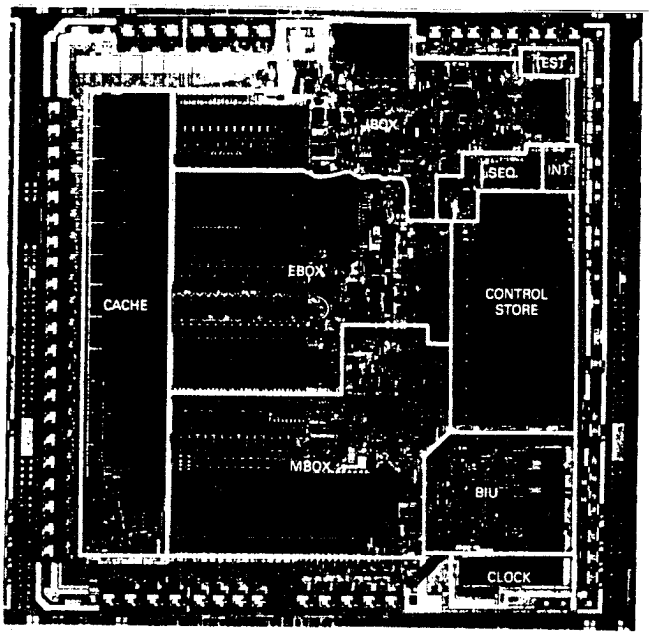


1975 1988

- **Approximately equal areas from ICs in 1961 and 1988.**



1968

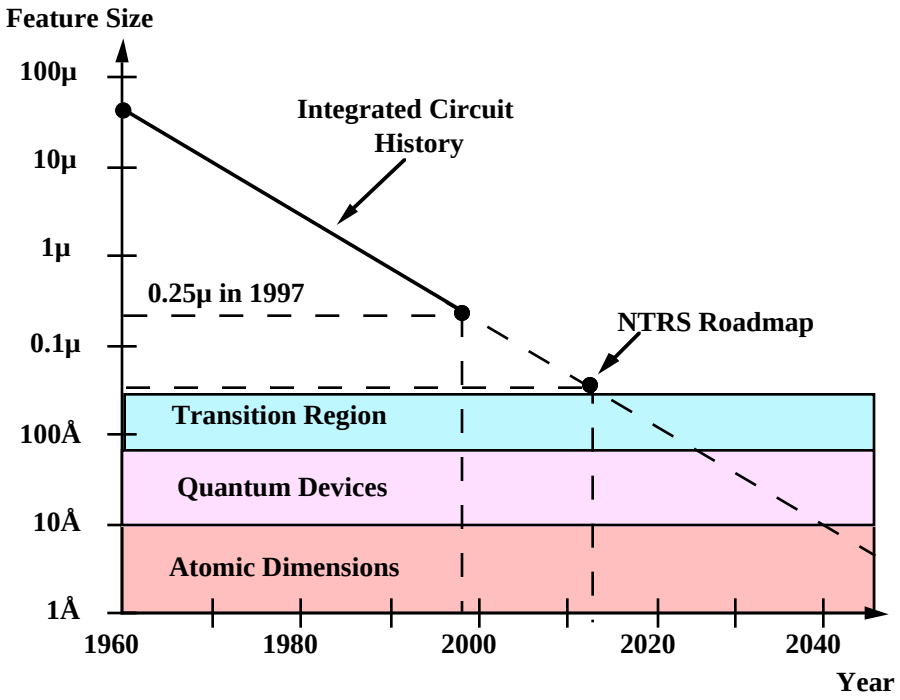


1988

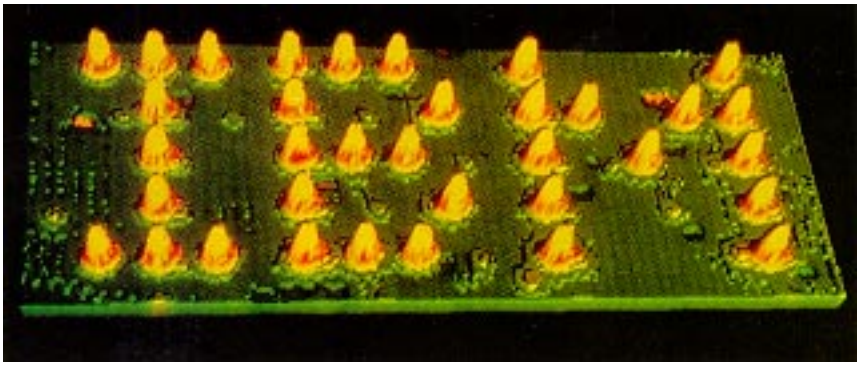
- **ICs manufactured in the 1960s and late 1980s.**

Year of 1st DRAM Shipment	1997	1999	2003	2006	2009	2012
Minimum Feature Size	250 nm	180 nm	130 nm	100 nm	70 nm	50 nm
DRAM Bits/Chip	256M	1G	4G	16G	64G	256G
DRAM Chip Size (mm^2)	280	400	560	790	1120	1580
Microprocessor Transistors/chip	11M	21M	76M	200M	520M	1.40B
Maximum Wiring Levels	6	6-7	7	7-8	8-9	9
Minimum Mask Count	22	22/24	24	24/26	26/28	28
Minimum Supply Voltage (volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6

- **1997 SIA NTRS (selected data)**



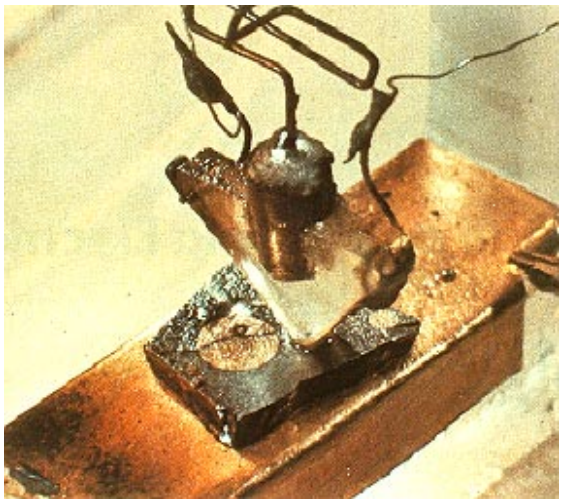
- **History and future projections for minimum feature size in silicon chips.**
- **Device limits appear today to be ≈ 250 Å channel lengths in MOS transistors.**



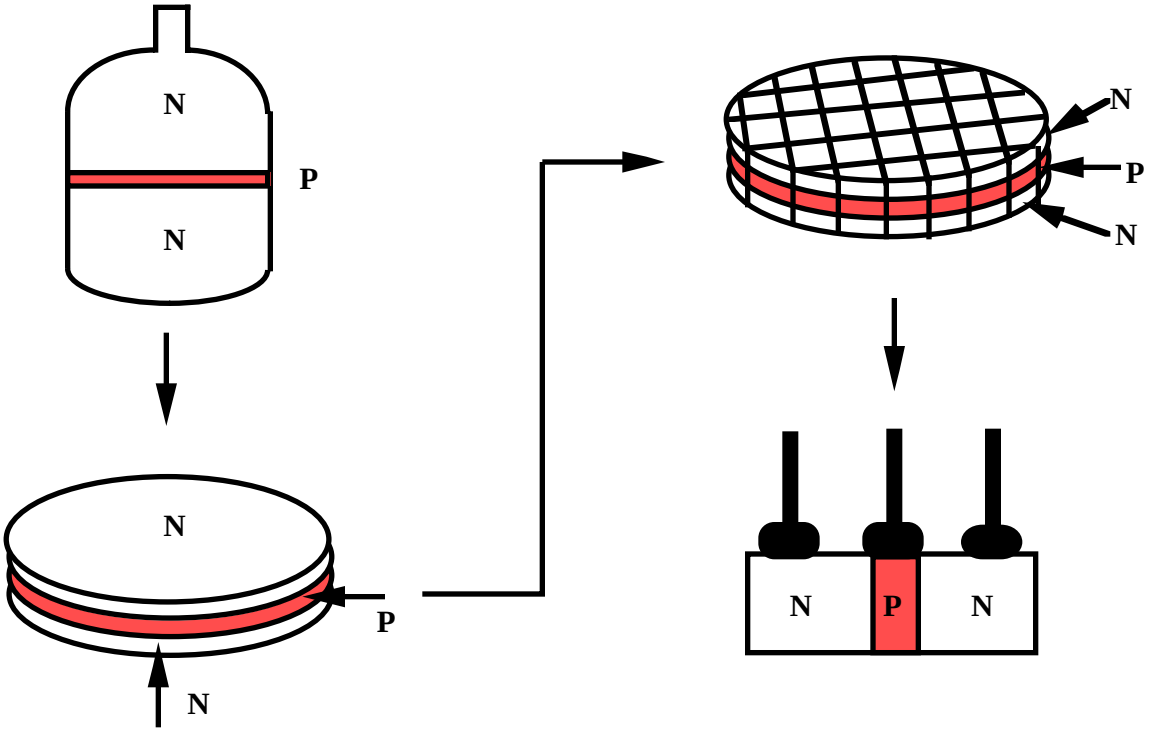
- **1990 IBM demo of Å scale “lithography”.**
- **Technology appears to be capable of making structures much smaller than currently known device limits.**

Historical Perspective

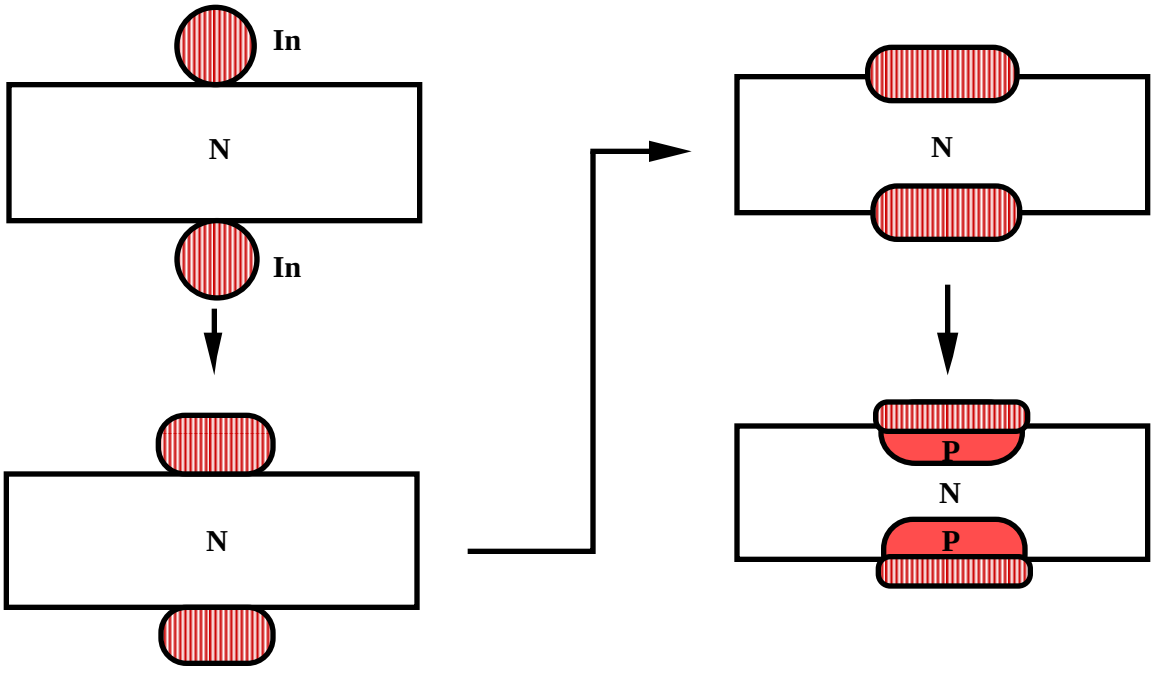
- **How did we get to today’s planar technology?**



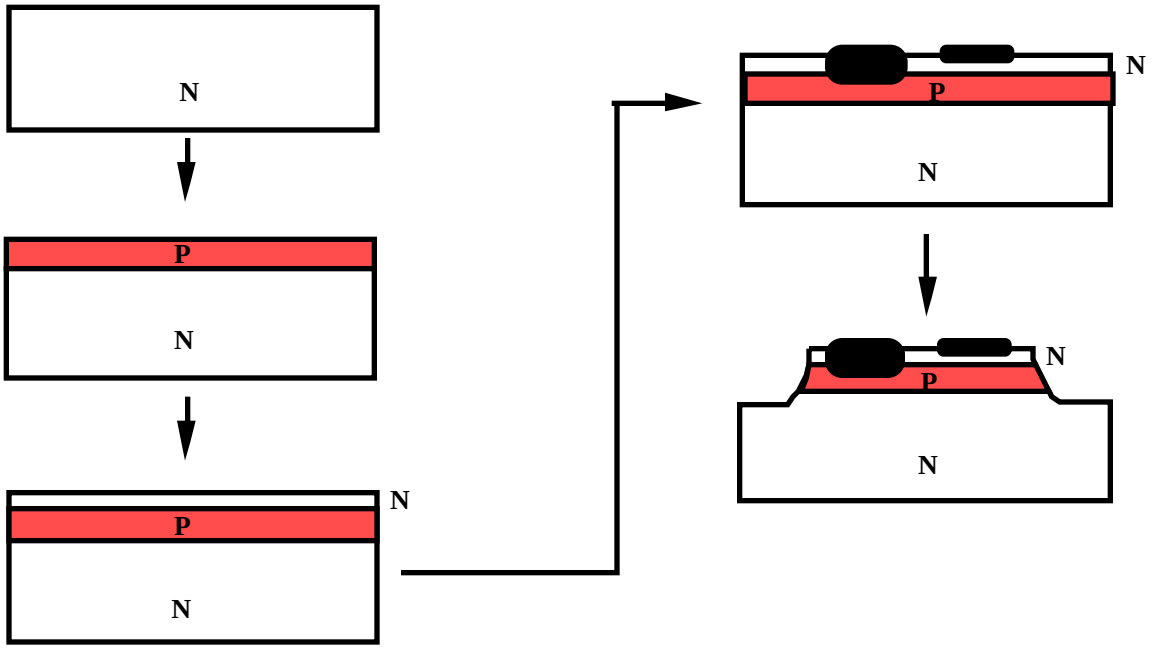
- **Invention of the bipolar transistor - 1947, Bell Labs.**
- **Shockley’s “creative failure” methodology.**



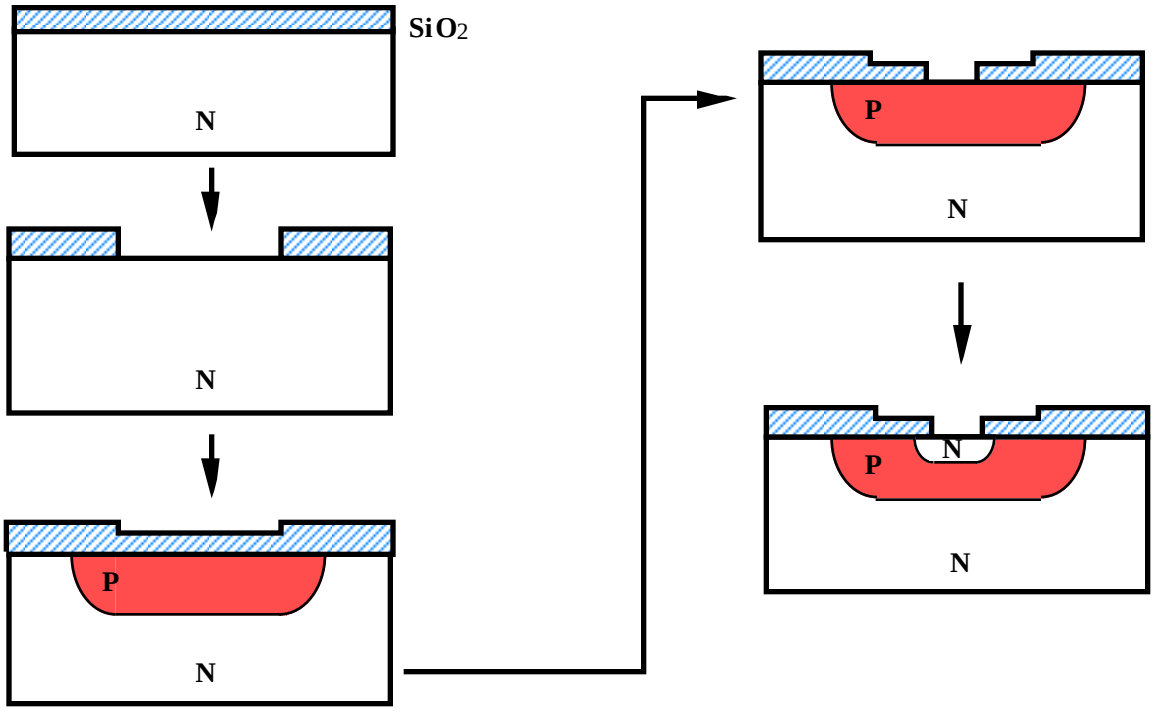
• **Grown junction transistor technology of the 1950s.**



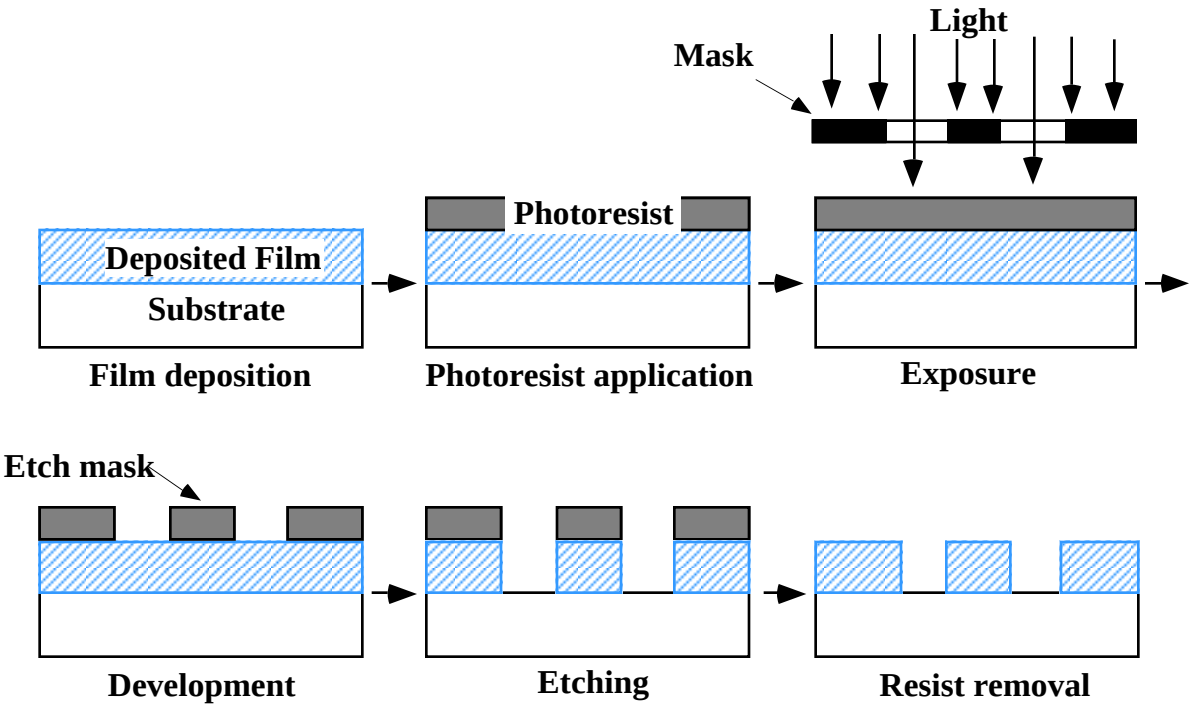
• **Alloy junction technology of the 1950s.**



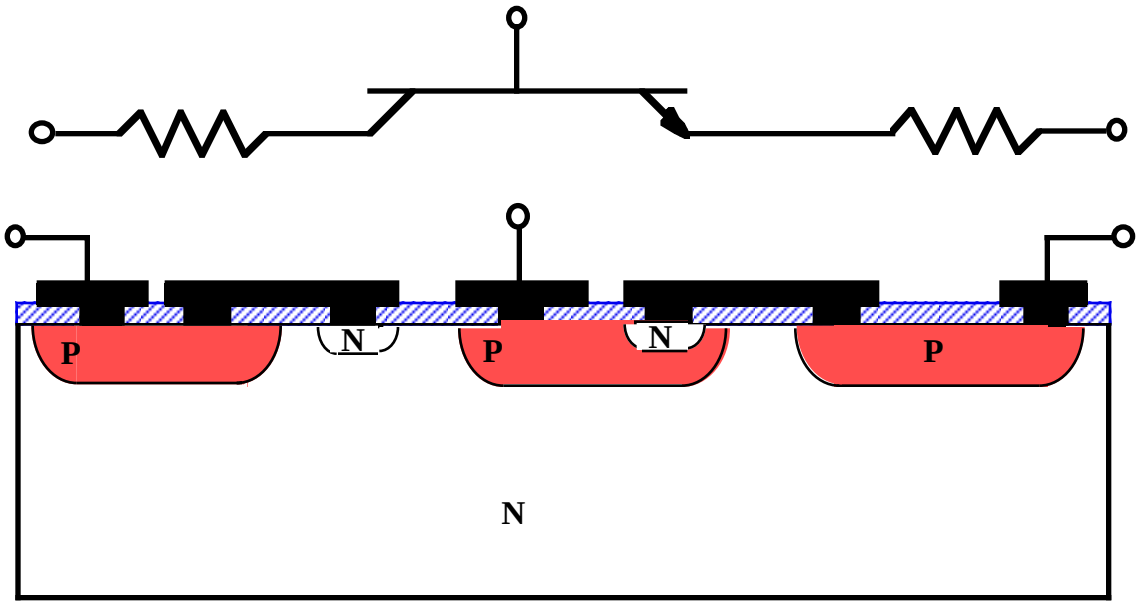
• **Double diffused transistor technology of the 1950s.**



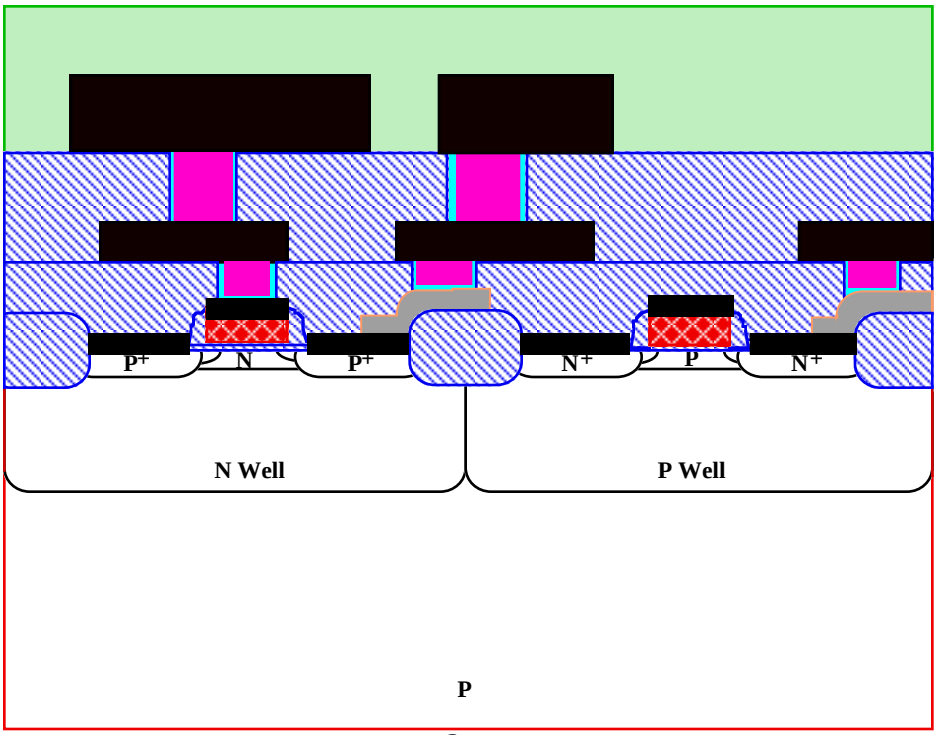
• **The planar process (Hoerni - Fairchild, late 1950s).**



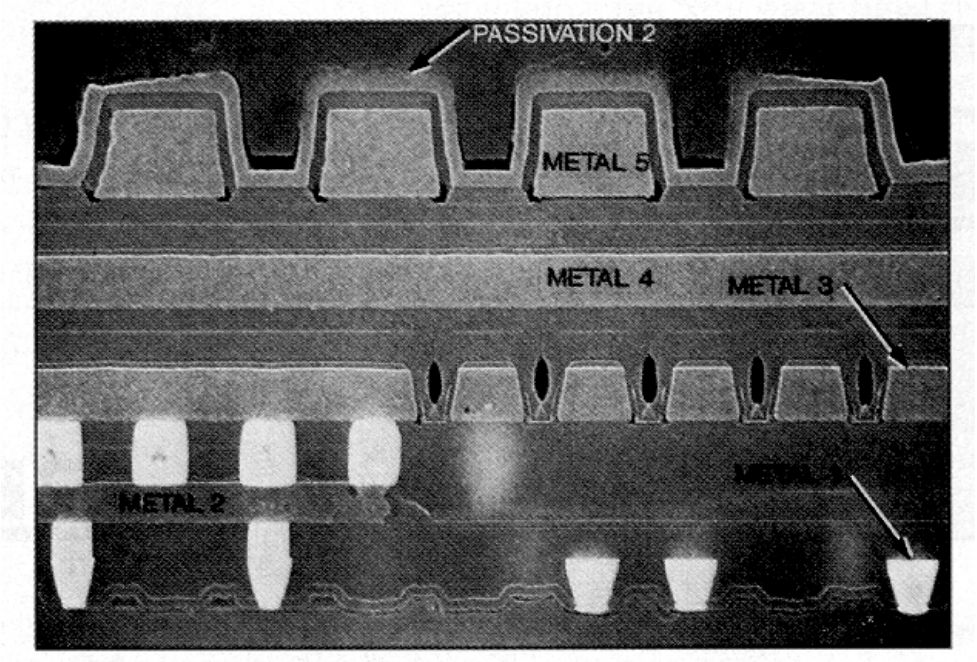
- **Basic lithography process which is central to today's chip fabrication.**



- **Lithographic process allows integration of multiple devices side by side on a wafer.**



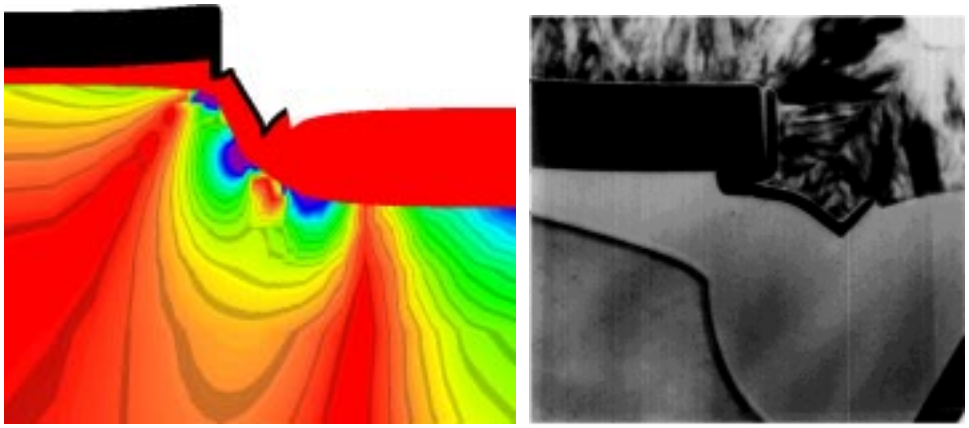
- **Schematic cross-section of a modern silicon IC.**



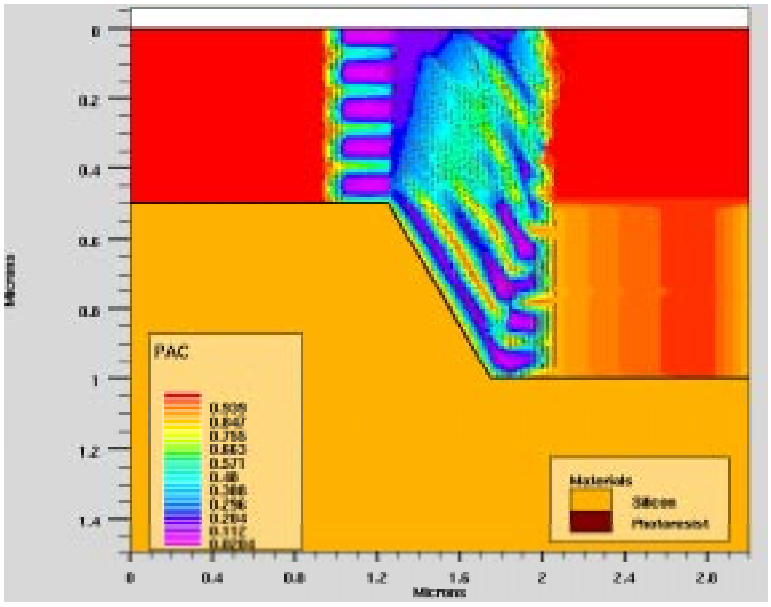
- **Actual cross-section of a modern microprocessor chip. Note the multiple levels of metal and the planarization.**

Computer Simulation Tools (TCAD)

- Most of the basic technologies in silicon chip manufacturing can now be simulated.
- Simulation is now used for:
  - Designing new processes and devices.
  - Exploring the limits of semiconductor devices and technology (R&D).
  - "Centering" manufacturing processes.
  - Solving manufacturing problems (what-if?)



- Simulation of an advanced local oxidation process.



- Simulation of photoresist exposure.

- **You should read the remaining material in Chapter 1 on semiconductor materials and devices. It will not be on HW assignments or exams in this class, but it will provide useful background.**