Exam #2 — EE 531
Winter 2003

The test is open book/open notes. Show all work. Be sure to state all assumptions made and check them when possible. The number of points per problem are indicated in parentheses. Total of 140 points in 6 problems on 6 pages. Assume $T = 300K$.

1. An MOS capacitor is made with a $p^+$ poly gate ($E_f = E_v$), a uniformly doped substrate with $N_d = 2 \times 10^{18} \text{cm}^{-3}$ and $t_{ox} = 2\text{nm}$. There is a substantial density of surface states such that $N_{ss}(E) = 10^{12}\text{cm}^{-2}\text{eV}^{-1}$ and $Q_{ss} = 0$ when $E_f = E_i$.

   (a) If $\psi_s = -0.2\text{V}$, calculate the applied gate voltage. (14)

   (b) What is the low frequency small signal capacitance that would be measured under these conditions (don’t forget the interface charges)? (10)
2. An nMOS transistor has $V_{FB} = -1.05\, V$ and $t_{ox} = 2\, \text{nm}$. The channel doping is small up to a depth $a$ and then the doping rises abruptly to $4 \times 10^{18} \, \text{cm}^{-3}$.

(a) What value of $a$ would give a long-channel threshold voltage of 0.5 V? (15)

(b) If $V_{gs} = 1\, V$, calculate $V_{ds}^{sat}$. Plot the charge density, electric field and band diagram versus vertical position in the channel close to the drain under these conditions. (16)
3. An nMOS transistor with uniform channel doping has $V_{FB} = -1.05V \pm 0.03$, $t_{ox} = 2 \pm 0.1\text{nm}$, $N_n = 2 \pm 0.1 \times 10^{18}\text{cm}^{-3}$, $W = 0.15 \pm 0.01\mu\text{m}$, and $L_{eff} = 0.07 \pm 0.01\mu\text{m}$ and is operated in system with $V_{dd} = 1.2 \pm 0.1V$. Assume mobility in inversion layer is given by value at edge of strong inversion.

What is the worst-case leakage current ($V_{gs} = 0$, $0 \leq V_{ds} \leq V_{dd}$)? Note that process variations can have multiple effects. Identify dominant effect in determining worst-case condition. (25)
4. We will compare the behavior of two similar silicon nMOS (p-substrate) devices at 300K. One of
the devices is a standard structure with channel region uniformly doped. The other has slightly
lower bulk doping and an addition shallow acceptor implant. For both transistors, the oxide
thickness, channel dimensions \((W, L)\), and threshold voltage are the same.

(a) Which has the preferable subthreshold slope factor? Explain. (8)

(b) Which device has the lower drain to body junction capacitance? Explain. (7)

(c) Which transistor will be more immune to reductions in threshold voltage due to short channel
effects? Explain. (7)
5. Consider a long-channel MOSFET transistor an $n^+$ polysilicon gate. The channel region is doped uniformly depth, but the doping varies laterally from the source to the drain as:

$$N_A = N_A^S, \text{ for } 0 < y < L/2$$

$$N_A = N_A^D < N_A^S, \text{ for } L/2 < y < L$$

(a) Give an expression for the threshold voltage. (8)

(b) Derive an expression for the linear drain current. (16)
6. It can be seen from the plots of mobility versus effective vertical field that the mobility increases and then decreases as the effective field increases.

(a) Why does the mobility drop for high vertical fields and why is the mobility nearly the same for all doping levels under these conditions? (7)

(b) Why does the mobility also drop as the field is reduced, particularly for heavily-doped channels? Note that the mobility drops substantially below the bulk mobility for a given doping. Hint: Think about the primary scattering mechanism limiting mobility under these conditions and how it changes as $E_f - E_v$ changes near interface. (7)