1. Problem 3.8 in text.

2. You are told by your process engineers that they can control doping concentration within ±5% and channel dimensions within ±0.02μm.

(a) Given these process variations, design an NMOS transistor with an n+ poly gate (φ_poly ≅ χ_s), 4nm thick oxide, deep source/drains, a very shallow threshold-shifting implant, and otherwise constant substrate doping to minimize the worst-case switching time under the constraint that the worst-case off-state leakage current is less than 1nA/μm (with V_{GS} = 0V and including DIBL). Assume that the power supply voltage is 2V (set to limit gate field to 5MV/cm) and that the switching speed can be approximated by

\[ W \left[ 4LC'_{ox} + (0.5\mu m)C'_j \right] V_{dd}/I_{DS}, \]

(C_j is junction capacitance for S and D) where I_{DS} is calculated from Eq. 3.76 for V_{GS} = V_{DS} = 2V and V_{SB} = 0. You have control over the substrate doping, implant dose (to shift V_T, ignore effect on mobility), and channel dimensions L and W. Use Eq. 3.66 in the text for short channel effects and DIBL and the model for channel length modulation from Eq. 3.97 (use E_{sat} = 2E_c, \( v_{sat} = 8 \times 10^6 \) cm/s). Use value of effective mobility calculated at the source.

(b) Test your design using Medici (remember to use worst-case analysis). You can modify the example used in previous homework. Suggest possible reasons for significant discrepancies. Test the switching speed first by just determining I_{DS}. Then use an output load consisting of a capacitor equal to 4WLC'_{ox} (fan-out of 4 equivalent transistors) in a transient simulation. Initialize the capacitor with a voltage equal to 2V and determine the time to discharge down to 0.5 V (roughly V_T).

3. Briefly describe (1-2 paragraphs) your plans for final project.