Homework #6 - EE 531

due 5/17/11

1. Consider an MOS capacitor with $x_{ox} = 3\,\text{nm}$, a p^+ poly gate doped with $N_a = 4 \times 10^{19}\,\text{cm}^{-3}$, a substrate uniformly doped with $N_d = 10^{18}\,\text{cm}^{-3}$ and negligible oxide charges.

   (a) Including poly depletion (use depletion approximation) and the finite thickness of the inversion layer (use appropriately simplified version of Eq. 2.154), derive an expression for $dQ'_I/dV_{GB} \approx dQ'_s/dV_{GB}$ in very strong inversion ($Q_I \gg Q_d$).

   (b) Using this expression, determine by what factor the inversion charge is reduced due to these two effects for $V_{GB} = V_T - 0.3V$ and $V_{GB} = V_T - 1V$, where V_T is defined by $\psi_s = 2\psi_B$. Which effect is more significant in each case?

2. (a) Using the charge sheet approximation, determine the first-order Taylor expansion of the maximum depletion charge around $V_{CS} = 0$. Show that using this approximation, the drain current matches the expression provided in class. What is the appropriate expression for $\alpha = m - 1$?

   (b) For a silicon-gate NMOS process,

$$\begin{aligned} N_a &= 5 \times 10^{18}\text{cm}^{-3} \quad \text{(uniform)} \\ t_{ox} &= 20\,\text{Å} \quad \text{(gate oxide)} \\ \phi_{MS} &= -0.95\,\text{volts} \\ Q'_{ox} &= 5 \times 10^{10}\text{cm}^{-2} \quad \text{(interface oxide charge)} \\ V_{BS} &= -1.0\,\text{V} \quad \text{(substrate bias)} \\ W/2 = L &= 100\,\text{nm} \end{aligned}$$

   Determine the value of α such that with $V_{GS} = V_{DS} = 1.5\text{V}$, the simplified model (with α) and the accurate model (with 3/2 power) predict the same drain current. Compare your result to the α value which is most accurate for small V_{DS} (answer to part (a)). Calculate the error between the models for $V_{GS} = 1.5V$, $V_{DS} = 0.8\text{V}$ using the values of α you calculated.

3. Using the structure of the first Sentaurus-Device MOSFET example:

   (a) Based on the simulation results, estimate V_T, m (extract two values, one from saturation voltage and the other from subthreshold slope in the absence of interface states), and $\mu C_{ox}/L$ (current is given per micron of width). Compare these values to calculations based on equations discussed in class.

   (b) If we consider a transistor to be off when $I_{ds} < 10^{-8} A/\mu\text{m}$, calculate the gate voltage required to turn off the gate (with $V_{ds} = 0.1\,\text{V}$) and compare to simulation results.

   (c) Modify and run these files to display a plot of the electron potential versus lateral distance from source to drain in the silicon very close to the Si/SiO_2 interface for the MOSFET biased in the cutoff, linear and saturation regimes. Comment on the results with respect to the barrier(s) seen by electrons in flowing from the source to the drain.

   (d) For the same bias conditions, plot the electrical potential as a function of depth (vertical distance) at $L/10$ (near source), $L/2$ and $9L/10$ (near the drain). Compare the voltages dropped across the silicon and the oxide to models used in class to predict MOSFET behavior.

   (e) On a 2D plot, view the electric field vector in the silicon under the same conditions as in (a). Is the gradual channel approximation a good one throughout the device? If not, where is it violated?

   (f) Analyze GIDL and channel avalanche breakdown by calculating substrate current as a function of V_{DB} for $V_{SB} = 0$ and $V_{GS} = -0.5$, 0, 0.5, 1.0 V.