Homework #7 - EE 531

due 5/26/11

1. Assuming that the dependence of the channel mobility on the vertical electric field is given by
$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \alpha \bar{\mathcal{E}}_{\text{vert}} \mu_0},$$
where $\bar{\mathcal{E}}_{\text{vert}}$ is the average of the vertical electric field at the Si-SiO_2 interface (depends on Q'_s) and just below the inversion layer (depends on Q'_d), determine an expression for the effective mobility as a function of $(V_{GS} - V_T)$, V_{SB} and V_{CS}. Is this model equivalent to any of the options provided with Sentaurus-Device (see manual)? If so which one(s) and under what condition(s)?

2. Compute the ballistic on-current for a modern transistor with the following parameters: $V_{DD} = 1.0\,\text{V}$, $t_{ox} = 1.2\,\text{nm}$, $V_T = 0.3\,\text{V}$ (Note that t_{ox} is actually an effective, electrical, thickness that accounts for the influence of the semiconductor capacitance and the depletion of the poly silicon gate). What fraction of the ballistic limit does the actual device deliver?

3. You are told by your process engineers that they can control doping concentration within $\pm 5\%$ and channel dimensions within $\pm 0.02\mu$m.

   (a) Given these process variations, design an NMOS transistor with an n^+ poly gate ($\phi_{poly} \cong \chi_s$), 4nm thick oxide, deep source/drains, a very shallow threshold-shifting implant, and otherwise constant substrate doping to minimize the worst-case switching time under the constraint that the worst-case off-state leakage current is less than 1nA/μm (with $V_{GS} = 0$V and including DIBL). Assume that the power supply voltage is 2V (set to limit gate field to 5MV/cm) and that the switching speed can be approximated by
   $$W \left[4LC'_{ox} + (0.5\mu\text{m})C'_j \right] V_{dd}/I_{DS},$$
   (C'_j is junction capacitance for S and D) where I_{DS} is calculated from Eq. 3.77 for $V_{GS} = V_{DS} = 2V$ and $V_{SB} = 0$. You have control over the substrate doping, implant dose (to shift V_T, ignore effect on mobility), and channel dimensions L and W. Use Eq. 3.67 in the text with $a = 0$ (as in Lundstron notes) for short channel effects and DIBL and the model for channel length modulation from Eq. 3.101 (use $\mathcal{E}_{sat} = 2\mathcal{E}_c$, $v_{sat} = 8 \times 10^6$ cm/s). Use value of effective mobility calculated at the source.

   (b) Test your design using Sentaurus using appropriate models (remember to use worst-case analysis). You can modify the example used in previous homework. Suggest possible reasons for significant discrepancies. Test the switching speed first by just determining I_{DS}. Then use an output load consisting of a capacitor equal to $4WLC'_{ox}$ (fan-out of 4 equivalent transistors) in a transient simulation. Initialize the capacitor with a voltage equal to 2V and determine the time to discharge down to 0.5 V (roughly V_T).

4. Briefly describe (1-2 paragraphs) your plans for final project.